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THESIS

INTRODUCTION OF A CURRENT WAVEFORM,
WAVESHAPING TECHNIQUE TO LIMIT CONDUCTION
LOSS IN HIGH-FREQUENCY DC-DC CONVERTERS
SUITABLE FOR SPACE POWER

by

Douglas P. Miller

June 1990

Thesis Advisor:

Gerald D. Ewing

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Introduction of a Current Waveform, Waveshaping Technique to Limit Conduction
Loss in High-Frequency DC-DC Converters Suitable for Space Power

by

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Lieutenant, U.S. Navy
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Submitted in partial fulfillment of the
requirements for the degree of

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ABSTRACT

Space power supply manufacturers have tried to increase power density and construct smaller, highly efficient power supplies by increasing switching frequency. Incorporation of a power MOSFET as a switching element alleviates switching loss. However, values of $R_{DS(on)}$ (drain-to-source resistance in the on-state) for MOSFET's are of such magnitude to produce greater on-state losses than an equivalent BJT operated in saturation. This research serves to introduce a design concept, pertinent to low-voltage relatively-high-current applications, that minimizes the peak current through the switching element in order to reduce average power loss. Basic waveforms produced by different PWM and resonant mode topologies were examined. Theoretical analysis reveals that a ramp-sine current waveform could cut conduction power loss by at least 18% over a conventional Buck switching converter. A 14V, 14W combination quasi-resonant Buck/ZCS, Quasi-Resonant Buck dc-dc converter with an unregulated input voltage of 28 V was built for simplicity to demonstrate one particular waveshaping technique. This converter represents a useful example of an actual circuit which is capable of producing the desired ramp-sine switch-current waveform. Final results confirm improvement in conduction loss enhancing existing power MOSFET technology for use in dc-dc power conversion.

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I. INTRODUCTION

A complete satellite power system consists of a multipanel solar cell array, a rechargeable battery, voltage limiting elements, and power conditioning devices such as voltage regulators and direct current-to-direct current (dc-dc) converters. Spacecraft power systems are involved in the efficient collection, transformation, and distribution of accessible solar, chemical and/or nuclear energy into electrical power for consumption by other systems and payloads. Advancing technology for spacecraft has placed increased demands on components of the system itself. Use of improved power electronics for power conditioning is today a necessity. The power conditioning aspect associated with electrical power systems has become the heart of all spaceborne craft. Power control electronics are responsible for effectively fulfilling the engineering power management function (power flow control, balanced energy management of multiple power sources and energy storage elements, autonomy of system operation during all mission phases, and elimination of potential mission critical failure modes) onboard all orbiting platforms. [Ref. 1:p. 391]

The power distribution of energy to other systems and payload equipment alike in an unregulated bus is accomplished through decentralized dc-dc converters. Designers distribute raw unconditioned dc power and regulate the voltage at the point of use in order to build redundancy into a system. Large numbers of converters are therefore necessary to meet all voltage and power requirements present in a spacecraft.

Spacecraft power systems were for a long time considered of secondary importance, considered to be very conventional in nature, and hence received minimal

attention during the thought process from which development of the satellite system architecture occurred. A study conducted on eight Jet Propulsion Laboratory funded programs, Mariner Mars 1964 through Galileo 1986, reveals in Figure 1.1, that about 30% of total spacecraft weight is concentrated in packaged electronics [Ref. 2:pp. 134-135]. With the greatest potential for spacecraft mass savings coming in this area over time, as proven in Figure 1.2, the impact of efficient circuit operation and physical realization of electronic power subsystems has become readily apparent. The call for improved efficiency and higher switching frequencies has renewed interest in both resonant and pulse width mode (PWM) technologies.

One of the most significant opportunities for improving power density in a dc-dc converter (as illustrated in Figure 1.3) comes in the area of the switching element. Power Metal-oxide Semiconductor Field Effect Transistors (MOSFETs) allow dc-dc converter operation to take place at higher switching frequencies, using relatively simple drive circuitry to add to system reliability. However, this device cannot operate without loss and is impaired by certain kinds of dissipative losses.

Power losses in a dc-dc converter are comprised of both switching losses and conduction losses. Switching losses increase in direct proportion to frequency. Each time the switching element is turned on or turned off, as demonstrated in Figure 1.4, a proportional amount of energy is dissipated. The more frequently the device is operated, the greater the power loss. At the other end of the spectrum exist conduction losses. This form of energy dissipation represents an almost constant loss, strictly dependent upon the converter load and the on-resistance characteristic of the particular MOSFET chosen as the switching element [Ref. 3:p. 322]. MOSFETs are capable of fast switching, but are relatively high in conduction loss.

The motivation for moving towards higher switching frequencies as shown in Figure 1.5 is to reduce the volume of the reactive energy storage elements, which

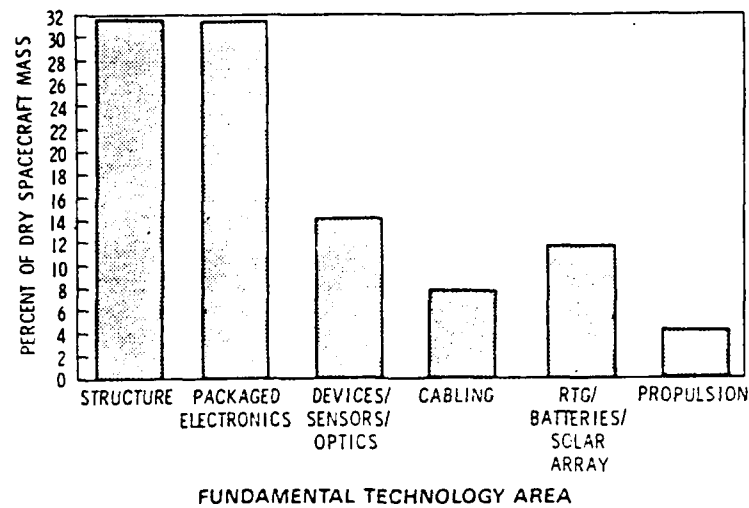


Figure 1.1: Weighted Average of Spacecraft Mass by Technology [From Ref. 2]

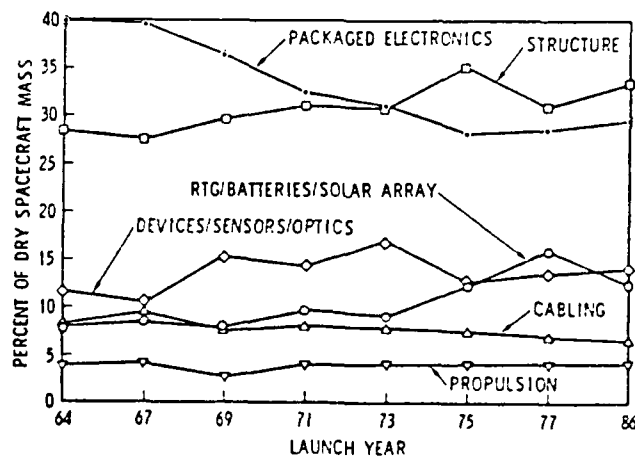


Figure 1.2: Normalized Percentage of Spacecraft by Technology vs. Time [From Ref. 2]

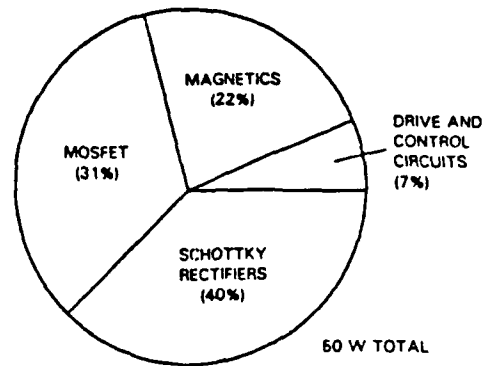


Figure 1.3: Relative Losses Within a 400 kHz DC-to-DC converter [From Ref. 3]

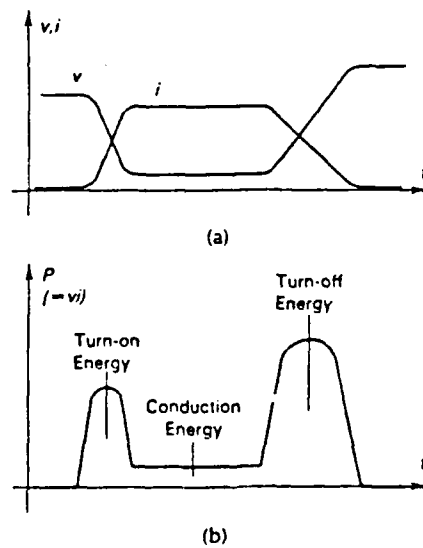


Figure 1.4: Power Semiconductor Switch (a) Voltage and Current Waveforms and (b) Dissipated Power Waveform [From Ref. 3]

comprise a major portion of a dc-dc converter. These elements become smaller in size at higher frequencies, because they need to store relatively less energy for shorter periods of time. For this savings to occur, the switching frequency must be raised from tens of kilohertz to hundreds of kilohertz [Ref. 2: p. 319]. Beyond this point, movement into frequencies in the megahertz range produces significantly less yield. Tradeoffs due to parasitic elements start to occur. [Ref. 3:p. 319, Ref. 4:p. 61, Ref. 5:p. 362]

Power conversion designs employing conventional PWM dc-dc converters are, however, besieged by switching losses at higher frequencies. PWM converters have been perfected to operate most efficiently at an optimal switching frequency range between 30-50 kHz [Ref. 6:p. 58]. In a square-wave operation, each time the switching element is turned on or off, and current or voltage is interrupted, energy is dissipated in the form of heat. Worry over a proper thermal design and the size of the heat sink increases. To remedy this situation and alleviate switching loss, quasi-resonant dc-dc converters have recently been developed for use. Experimentally, this technique using power MOSFETs has been proven successful for higher frequencies up to approximately 10 MHz [Ref. 4:p. 61]. This type of dc-dc converter increases efficiency as it separately improves reliability by alleviating switching stresses.

To achieve higher power system density and reduce the size and cost of the power conversion subsystem designs, design engineers have, in their research and development efforts, focused most of their attention on:

- higher switching frequencies,
- higher levels of circuit integration, and
- improved thermal performance [Ref. 3:p. 319].

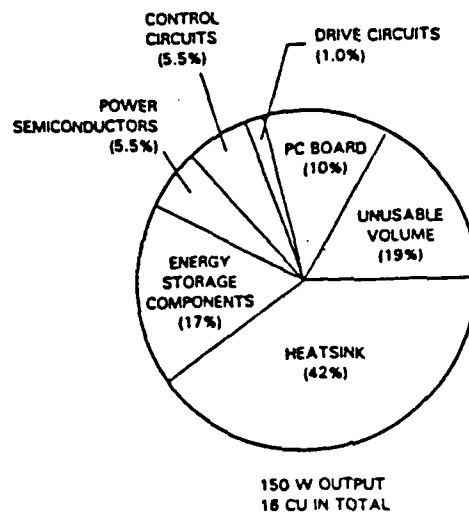


Figure 1.5: Relative Portions of a Space Consumed in a DC-DC Converter Operating at 400 kHz [From Ref 3.]

However, it is the intent of this research to concentrate specifically on conduction loss. On a percentage basis, conduction losses are more prevalent in instances when power is supplied at low voltages and high currents, as in satellites. This thesis, for two reasons, is used to develop an engineering scheme which creates a switch-mode current waveform that represses conduction loss in a power MOSFET.

First, when operating a conventional PWM dc-dc converter, a trade-off exists in this technology between greater on-state losses and lower switching type transient losses. Power MOSFETs are characterized by their fast switching speeds and a relatively large forward drop in the on-state. As expected, a Bipolar Junction Transistor (BJT) has a significantly less total power loss at low frequencies while the performance of a power MOSFET is greater at high frequencies. Any improvement in the form of the resulting switch-mode current waveform put through the

semiconductor switch will lessen the detrimental effect produced by conduction voltage drop in either case. However, the movement in the point of intersection (the "crossover point") between two curves showing the total power loss per unit area in these two types of transistors caused by a reduction in on-state losses would prove to be more instrumental in a majority carrier device functioning at a low frequency and low voltage. A combination of either two or three ZCS, quasi-resonant dc-dc converters would produce this effect and provide a boost in power density. This in-turn would reduce the symptom of higher resonating rms current, which would in the end cut conduction loss during the switch-on time interval.

Secondly, to a lesser extent, use of a ZCS, quasi-resonant technique would offer the consideration of extra power transferred per switching cycle without an increase in EMI.

The choice in this design is not to ameliorate component quality (e.g., MOSFET on-resistance) or to employ a very heavy gate overdrive to reduce on-voltage losses, but to concentrate on improving the behavior of the current waveform through the converter switching element itself. This research re-examines the basic features of both the Buck PWM and ZCS, Quasi-Resonant dc-dc converters to develop an ideal step-down converter topology. Combination of the best features of each type of converter is targeted to produce an optimal circuit design with the following characteristics in mind:

- low conduction losses due to use of a proposed waveshaping technique,
- higher operating efficiency,
- improved power density to lessen power demand requirements and reduce the physical size of the overall power system itself.

- one switching element,
- simple control circuitry,
- reduced radiation by employing a zero-current switching strategy,
- improved converter reliability and less stringent thermal design, which implies reduced switching stresses and switching losses,
- faster dynamic response from use of a power MOSFET.

Discussion in subsequent chapters begins by qualitatively developing a numerical method to compensate for on-resistance loss generated within the switching element. A technique used to minimize peak current through current waveform shaping is brought forward.

Chapter III is used next to present the different categories of power conversion alternatives available to the power electronics engineer today. Each major type of power supply is discussed concentrating on its ability to efficiently regulate supplied electrical power and control power dissipation losses. In particular, the basic operational theory and circuit analysis of both the PWM Buck dc-dc power converter and Quasi-Resonant, ZCS dc-dc power converter are given. This serves to introduce the parameters which affect boundary conditions and influence the dc conversion ratio in each circuit. The analysis is presented in a practical, easy-to-understand manner, in order to comprehend how the various modes and waveforms are produced.

The impact behind the selection of the switching element is judged in Chapter IV. The critical characteristics involved in the performance of POWERMOS transistors are purposely deliberated.

The last chapter outlines the theoretical process involved in the development of a ramp-sine current waveform. Certain design specifications are given. Specific

equations which dictate the exact relationship between the peak values of the two individual current waveforms are identified. As a practical example, the ramp-sine current waveform is produced from its brassboard model. The modes of the resulting circuit are illustrated.

The remaining portion of the chapter deals with an evaluation of dissipative losses from the operational circuit. As a result, a final comparison is made between the magnitude of the relative values of conduction loss which exist between different current waveforms.

II. GENESIS OF A NEW POWER CONVERSION STRATEGY

Both the passive and active components affect the overall mass, volume, and efficiency of a dc-dc converter. Analytical evaluation of the power losses associated with these elements therefore becomes necessary to achieve an optimal power system configuration.

Relatively speaking, as previously shown in Figure 1.3, the second highest power loss in a dc-dc converter comes in the activation of the primary power switch. Losses in the semiconductor device can reduce overall converter efficiency by 5-10% [Ref. 3:p. 322]. The seriousness of the loss is amplified and becomes significant as efficiencies begin to approach 90%.

The power dissipated, P_L , in a converter circuit is due to a combination of conduction and switching losses occurring in the switching element at turn-on and turn-off. Expressing these losses in their equation form leads to,

$$P_L = P_{cond} + P_{sw} \quad (2.1)$$

where

- P_{cond} = Total amount of conduction loss due to non-zero on-resistance, $R_{DS(on)}$, during switching element on-time.
- P_{sw} = Total amount of switching loss due to power dissipated in the switching element during both turn-on and turn-off times, and the type of load switched.

Attempts to further reduce dc-dc converter size and increase power handling density has led to much research using higher frequencies to eliminate switching losses. However, first and foremost, research in this section qualitatively seeks to demonstrate a means to compensate for on-resistance related losses. Assuming a fixed blocking voltage, on-state current, and device area, Figure 2.1 clearly demonstrates the limit conduction losses have placed on power MOSFET devices today. As switching frequencies extend into the 10 MHz frequency range and parasitics are explicitly incorporated into topological designs, emphasis on conduction losses can be expected to escalate rapidly [Ref. 5:p. 363], [Ref. 8:p. 12].

A. WAVESHAPING TO LIMIT POWER LOSSES

1. Conduction Losses

Manipulation of the current waveform through the converter switching element to control the conduction power loss is founded upon the following principles. First, the average amount of charge, Q , that a switching element can transfer in a prescribed amount of time, τ , is given by,

$$Q = \int_{t_1}^{t_2} i(t)dt \quad (2.2)$$

where $i(t)$ is the switch-current waveform under consideration. If τ is fixed, the maximum amount of charge attainable is strictly dependent upon the quantity of current, $i(t)$, present. Figure 2.2 represents three basic current waveforms with identical values of τ . In each case, peak current is expressed in terms of normalized charge, Q , divided by on-time, τ . As shown, the rectangular waveform most effectively supplies the desired amount of charge for the lowest value of peak current, I_p .

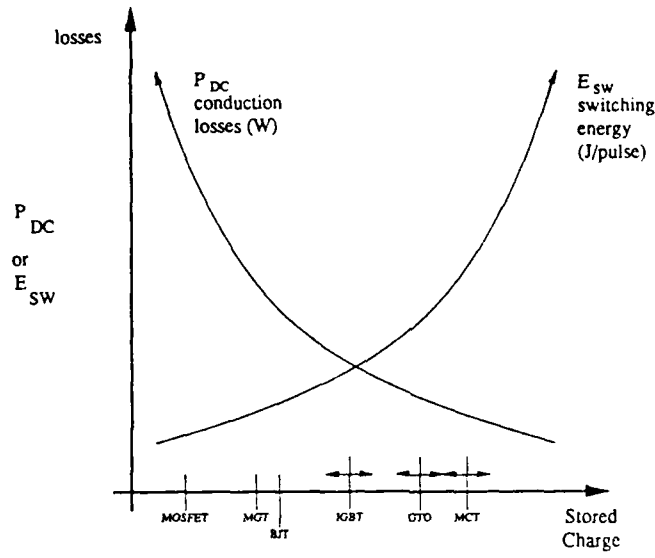


Figure 2.1: Qualitative Plot of Conduction Losses and Switching Energy Versus the Amount of Stored Charge [From Ref. 7]

Secondly, the average power dissipated by the switching element in the same cycle is proportional to,

$$P_{cond} = \frac{R_{DS(on)}}{T} \int_{t_1}^{t_2} i^2(t) dt \quad (2.3)$$

or

$$P_{cond} = f_s \tau I_{D(on)}^2 R_{DS(on)} \quad (2.4)$$

where

- τ = Switching element on-time,
- T = Switching period,
- f_s = Switching frequency.
- $I_{D(on)}$ = On-state drain current,

- $V_{DS(on)}$ = On-state drain-to-source voltage, and
- $R_{DS(on)}$ = Drain-to-source voltage in the on-state.

If $R_{DS(on)}$ and T are assumed to be equal to one in value, the power consumed by the conduction process is strictly dependent upon the current as a function of time squared. Control over this parameter is vitally important, and hence becomes the dominating theme behind the development of a waveshaping technique. Using the ramp function found in Figure 2.2 as an example, substitution of $i(t) = (I_p/\tau)t$ into Equation 2.3 yields

$$P_{cond} \approx \frac{\tau}{3} I_p^2, \quad (2.5)$$

an equation for power loss in terms of peak current and device on-time. Replacement of peak current in Equation 2.5 with an appropriate value of normalized charge produces figures for accompanying values of current and power. Results recorded in Table 2.1 prove, in this instance, that a ramp like current waveform is 33% less efficient than a rectangular waveform having a Q of one. Similarly, if the same logic is applied again, an expression can be developed for any half-sinusoidal current waveform as a function of time using,

$$i(t) = \int_0^{\tau_m} \sin\left(\frac{\pi t}{\tau_m}\right) dt \quad (2.6)$$

where τ_m is the half period of the m^{th} sinusoid in question and m is the integer number value of the particular waveform under consideration.

In contrast, a singular sinusoidal current waveform as shown in Table 2.1 can be expected to realize a 7.43% improvement in conduction loss over the ramp current waveform.

In order to experiment with different combinations of waveforms and to extend this analysis one step further, an optimization routine entitled ZXMIN was

TABLE 2.1: Waveform Results

WAVEFORM	I_p	P	Q	% REDUCTION RAMP
Ramp	2.000	1.333	1.0	0.00
Sine	1.571	1.234	1.0	7.43
Sine-Sine	1.395	1.147	1.0	13.95
Ramp-Sine	1.388	1.086	1.0	18.60
Sine-Sine-Sine	1.372	1.302	1.0	2.33
Ramp-Sine-Sine	1.171	1.001	1.0	24.90

used to lessen the prodigious amount of calculations involved. This algorithm, which is a part of the IMSL library, uses a quasi-Newton method to locate the minimum of a function $f(x)$ of N variables, $x = (x_1, x_2, \dots, x_n)$. By squaring the sum of the different current waveforms in question and integrating over the switching element on-time interval, a function proportional to the average power of the combined waveforms is derived. Applying ZXMIN produces an output vector X of length N . Vector X contains N final parameter estimate values, as determined by ZXMIN, that causes the power function to be a minimum. Each estimate represents the current amplitude and period required to minimize average power, P , at a Q equal to one for each combination. Appendix A is used to give a complete explanation of the IMSL routine ZXMIN. Also, present in Appendix A are the graphical results to the six different current waveforms analyzed.

Table 2.1, from the calculations performed in Appendix A, lists for each current waveform the minimum power, P , and associated current value, I_p , required

to produce a charge, Q , of one. The current I_p represents the resulting minimum peak current from the sum of m different waveforms being added together. Utilizing the ramp waveform as a benchmark, the particular combination of the ramp, sine, sine waveforms is most advantageous. A 25% reduction in conduction power loss is obtainable in comparison to the ramp waveform alone.

2. Switching Losses

Switching losses in a power MOSFET can be calculated using,

$$P_s = f_s \left[I_{D(on)} V_{DS(on)} \int_0^{t_{s1}} \left[\frac{t}{t_{s1}} \left(1 - \frac{t}{t_{s2}} \right) \right] + I_{D(on)} V_{DS(on)} \int_0^{t_{s2}} \frac{t}{t_{s2}} \right] dt \quad (2.7)$$

$$= f_s I_{D(on)} V_{DS(on)} \left[\frac{2}{3} t_{s1} + \frac{t_{s2}}{2} \right] \quad (2.8)$$

where

- t_{s1} = Current rise time, and
- t_{s2} = Current fall time.

Higher operating frequencies imply proportionally greater energy losses. When switching frequency is increased, larger heat sinks are required in dc-dc converters as the fixed amount of power dissipated during each cycle is repeated more often. Hence, switching losses limit dc-dc converter size. [Ref. 3:p. 322, Ref. 9:p. 4.5]

The results found in Table 2.1 are promising and a discovery of this nature may have other possible ramifications as well. Being able to construct a current waveform containing sinusoidal elements would constitute the creation of a zero-current-switching waveform. Turning the switching element on and off at zero current would not contribute, but assist in reducing both switching losses and

switching stresses. Thus, additional and unexpected gains in power density, efficiency, and reliability could be achieved in low voltage power applications. [Ref. 10, Ref. 11:p. 377-378]

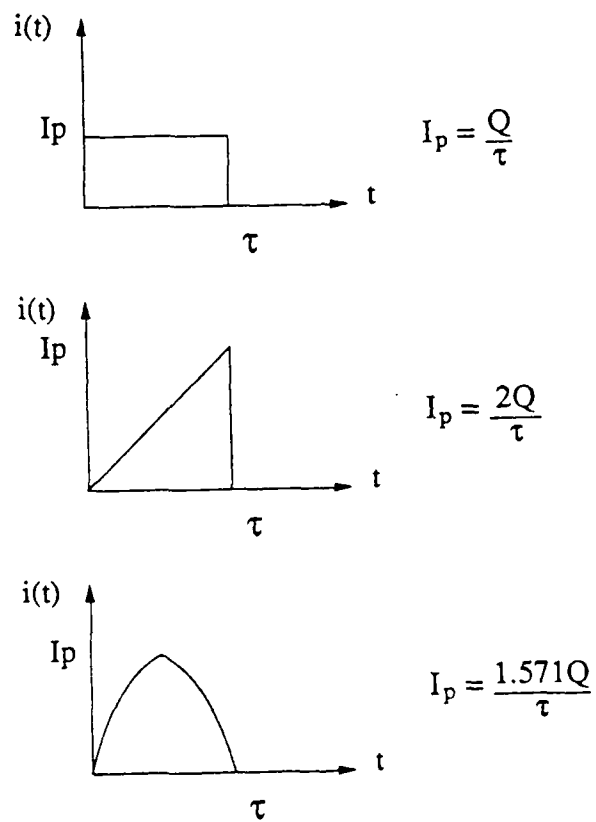


Figure 2.2: Hierarchy of Basic Current Waveforms as a Function of Charge, Q , and Switch on-time, τ .

III. POWER CONVERSION ALTERNATIVES

The concept of both linear and switch-mode power supplies is not new. As illustrated in Figure 3.1, there are several different types of power supplies available that will allow a design engineer to transform dc at one voltage level to dc of another voltage level. Over the years, the array of differences in voltage and current requirements specified for different applications has produced a variety of tailor-made dc-dc converters specially designed to meet this indigence state.

In a MOSFET, where conduction loss is

$$P_{cond} \sim I_{D_{rms}}^2, \quad (3.1)$$

the drain current, I_D , must be as small as possible to achieve highest efficiency. This chapter serves to examine how peak drain current through the switching element varies in two selected topologies.

The discussion begins with an investigation into the approach used in both linear and non-linear power supplies (square and sine-wave) to achieve voltage regulation in dc-dc power conversion; characteristic voltage and current waveforms are then explored to understand their waveshaping *modus operandi*. Today's superior high-frequency semiconductor devices permit active waveshaping to be employed as a methodology to better control and process power. Active waveshaping typically increases power density by extirpating most of the weight and volume normally dedicated to low frequency filter elements. Completion of this study is used by the author to verify that the current waveforms for the Buck and ZCS, quasi-resonant

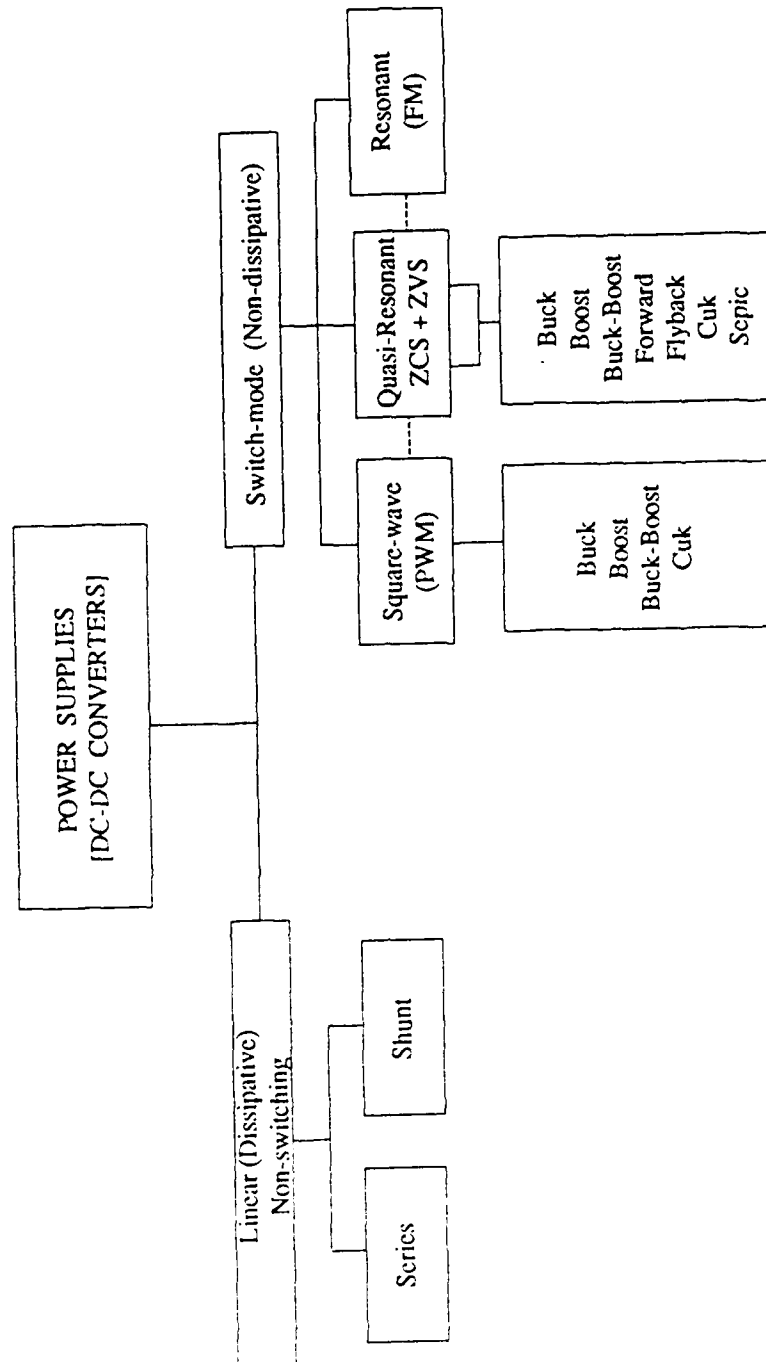


Figure 3.1: Classification of DC-DC Converter Power Supply Technology

dc-dc power converter topologies are appropriate for use in the framework of a dc-dc converter design. A model is developed for each converter type chosen which analyzes their structural properties and resulting voltage and current waveforms.

A. DISSIPATIVE OR LINEAR POWER SYSTEMS

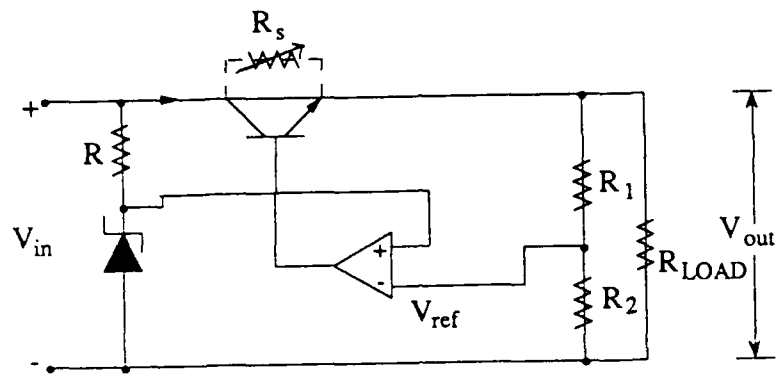
In the basic design of a linear power supply, as shown in Figure 3.2, the converter uses a series linear element, usually a transistor operating in the continuous conduction mode, to act as a variable resistor to control and regulate the output voltage. The voltage across the pass transistor is always equal to the difference between the input and output voltage. In the linear mode of operation, dissipation in the controlling element is high and converter efficiency is low (30-60%). The linear regulator circuit provides precise line and load regulation required at the output of the supply. Although simple in design, this regulator type possesses no waveshaping capability. Hence, both the series and shunt dissipative regulators are of little use to the design engineer in reducing system losses.

B. NON-DISSIPATIVE OR SWITCH-MODE POWER SYSTEMS

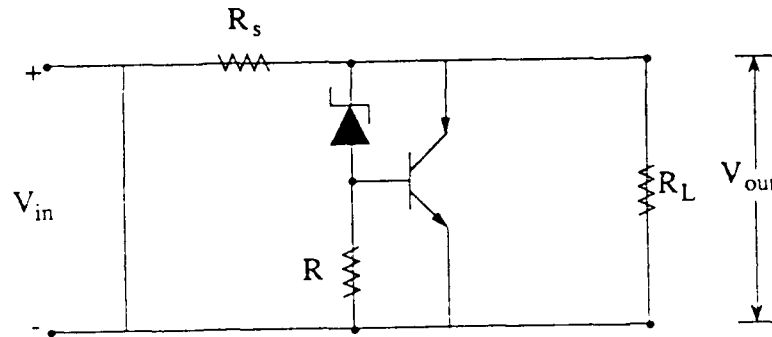
There are three separate classes of switch-mode converters available for use, they are:

- Square-wave.
- Resonant, and
- Quasi-resonant.

Classically, each type of switch-mode converter is composed of a power handling device arranged in tandem with a distinctive number of passive energy storage elements, inductors and capacitors, to form a unique topology capable of transforming



(a)



(b)

Figure 3.2: Linear DC-DC Power Systems: (a) Series Regulator, (b) Shunt Regulator

energy supplied by the source to the load. The power transistor is treated as an ideal switch. The kind of power transistor chosen is selected to operate in either its saturated (ON) or cut-off (OFF) mode to minimize power losses. The constant periodic changes between the two states makes these converters non-linear. Switch-mode converters possess the ability to use the fraction of time that the switch remains on (τ , t_{on} , DT, etc.,) in comparison to the switching period to regulate power flow to the load. The switching regulator obtains high efficiencies as a result of:

- its ability to vary the duty cycle to raise the switching frequency above the line frequency to reduce the volume of reactive components and limit power losses, and
- excellent closed loop load-transient response over wide ranges in load current [Ref. 12:p. 53].

Major internal losses, however, do exist from high currents flowing through the saturation resistance at transistor turn-on and transient switching losses occurring at higher frequencies.

The combination of high efficiency, small magnetics, and reduced switching stress has resulted in improved, more reliable power converters rated at 200 W, which are emerging with power densities approaching 1 kW/in³ at 98% efficiency [Ref. 13].

1. Square-wave Converters

As implied by Figure 3.3, a great variety of possible switch-mode topologies can be constructed using any particular combination of switches and storage components. However, only one out of the four of the most elementary converters, which are fundamental to all other derived dc-dc converters, is discussed here.

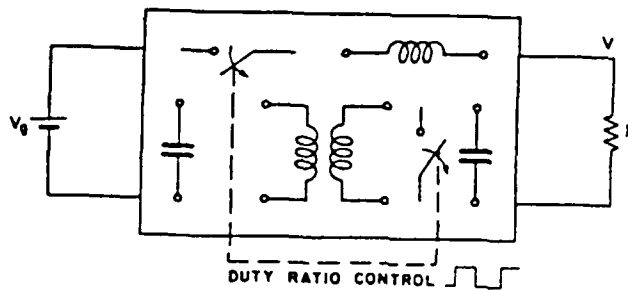


Figure 3.3: General Arrangement of Storage Components, Switches, and Low Pass Filter Elements in a Switch-mode DC-DC Converter [From Ref. 14]

The PWM controlled dc-dc converters, illustrated in Figure 3.4, operate in a switching mode rather than an analog mode to impress square waves of current and voltage onto power semiconductor switching elements. The desired dc output is controlled by use of a switching transistor, inductor or high frequency transformer, rectifier, and output filter network to properly regulate the voltage against changing line and load conditions. Typical square-wave converters process power at a rate of 20 to 500 kHz. Within this frequency range, the system is considered to be optimal in size, weight, reliability, and cost. Above this plateau, square-wave converters are completely overwhelmed by frequency related losses. At the cost of complexity, MOSFETs are generally used in resonant circuits to alleviate this condition.

a. Buck DC-DC Converter

(1) Operational Characteristics

The simplest and most fundamental configuration to understand is the basic Buck converter, illustrated in Figure 3.5. This switching regulator

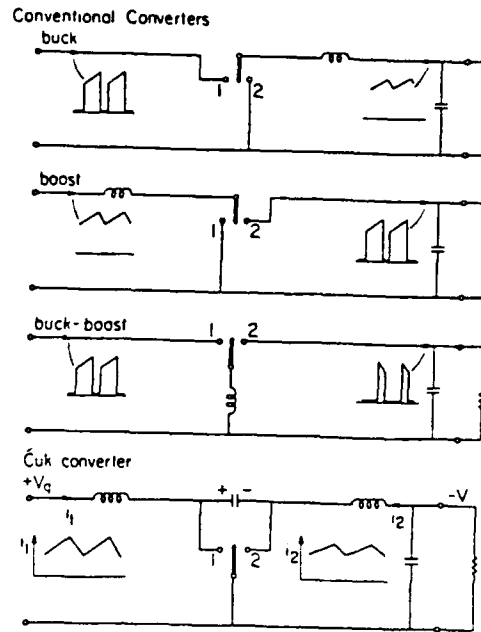


Figure 3.4: Input and Output Current Waveforms of Basic DC-DC Converters [From Ref. 15]

is comprised of the following components: an ideal switch, sw , which can be realized in this case by the implementation of a BJT with a free-wheeling diode, D_1 ; a dc power source, V ; and a L-C filter used to reduce voltage ripple and provide a constant output, V_{out} , across the load, R_L . The value of C is chosen such that it is sufficient in size to ensure that the change in V_L (ΔV_L) is small. The diode and transistor used in this discussion are assumed to be ideal switching components.

In a Buck dc-dc converter, the regulated output voltage, V_{out} , is always less than the given range of the input, V . Using an integrated circuit controller, the output voltage, V_{out} , can be compared with a stable reference voltage to create an amplified error signal to generate either a PWM or Frequency Modulated (FM) waveform, which will control the switch-off period adequately.

During the switching cycle in a Buck dc-dc converter, switch, sw , as indicated in Figure 3.5(a) is periodically manipulated after a given amount

of time, τ , from position A to position B for time $T - \tau$. The circuit topology in Figure 3.6 results. When switch, sw , is placed in position A at the beginning of the cycle time, t_0 , the input voltage, V , is greater than the output voltage, V_{out} . This produces a constant voltage, $V_L = V - V_{out}$, across inductance, L . Diode, D_1 , is reverse-biased due to the polarity of input voltage, V . This forces all current to flow into inductor, L , and a voltage to build across capacitor, C . Inductor current, $i_L(t)$, ramps upward producing an output voltage across the load with a polarity in the direction as shown in Figure 3.6. This process occurs approximately until the output voltage, V_{out} , exceeds a given reference voltage and the switch moves to position B . The peak current, I_p , developed in the inductor is directly proportional to the amount of time switch, sw , is turned-on.

Once a value of V_{out} is achieved, switch, sw , is turned-off or opened at time $t = \tau$. The voltage, V_x , immediately drops to zero volts and the stored magnetic energy in inductor, L , reverses its field polarity to preserve the flux created by the formerly applied emf, causing diode, D_1 , to become forward-biased. Diode D_1 , behaves as an automatic switch, able to commute inductor current. Current through inductor, L , begins to ramp downward as current is discharged into both the load, R_L , and filter capacitor, C . Note, that the output voltage polarity across the load, R_L , remains unchanged as the voltage out, V_{out} , remains constant.

At the end of the second time interval, either one of two different operational conditions can prevail. If the inductance current, $i_L(t)$, throughout the course of the switching cycle in Figure 3.7(a) never reaches zero, the circuit operationally is specified as acting in the *continuous conduction mode*. Inductor current, $i_L(t)$, is always some non-zero positive value. However, if all accumulated energy in inductor, L , is expended and dissipated in the load, capacitor C will be

forced to start its discharging process. This in turn will cause the output voltage to fall. The capacitor will completely discharge through the load due to diode, D_1 , positioning. At this point in time, switch sw will return back to position A and the process will repeat itself. A switch-mode converter in which the inductance current, $i_L(t)$, becomes zero during a portion of the switching process, as shown in Figure 3.7(b), is specified as operating in the *discontinuous conduction mode*. The minimum amount of time necessary for the load to dissipate the energy built up in the inductor for a given on-time, τ , is dictated by the size of the load requirement itself. As it will be shown in subsequent paragraphs, transition from a continuous to a discontinuous conduction mode can also be made a function of duty cycle, D , switching frequency, f_s , and inductance, L , as well.

(2) DC Voltage Conversion Ratio

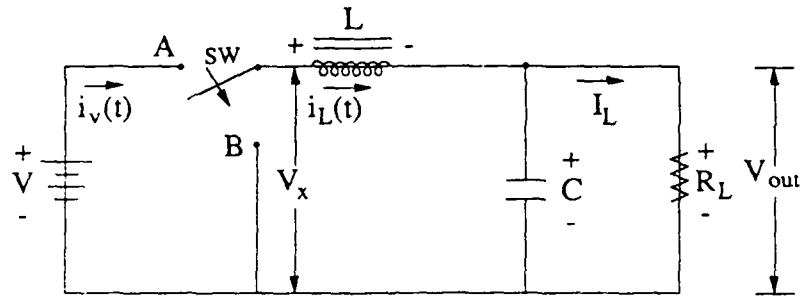
For any given design neglecting the voltage drop across the diode and the saturation voltage drop of the transistor in Figure 3.5, duty cycle, D , is defined as

$$D = \frac{\tau}{T} = \tau f_s \quad (3.2)$$

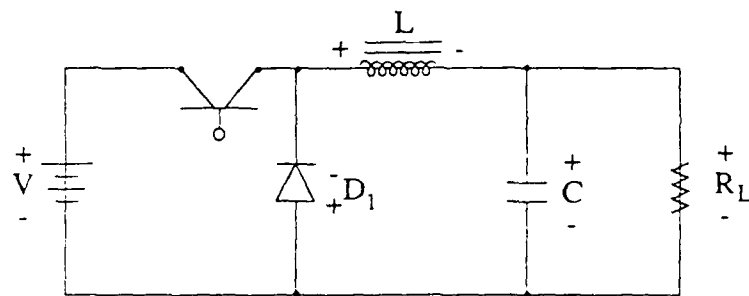
where

- τ = Switch on-time,
- f_s = Switching frequency, and
- T = Switching period.

Given the fact that the average voltage across an inductor over a complete period is zero, the volt-seconds stored in the inductor during interval, τ , must equal the volt-seconds released during the inductor discharge interval [Ref. 14:pp. 282-283, Ref. 17:p. 4]. Because of this, in the steady state the initial and final values of

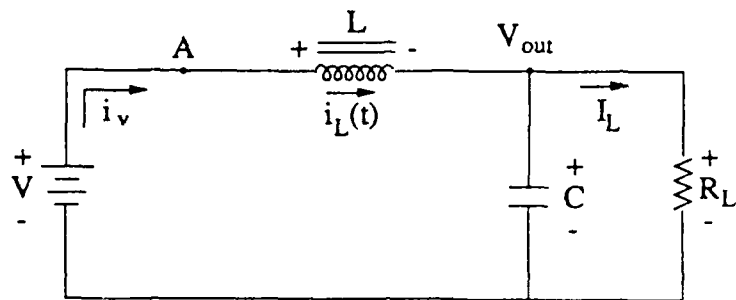


(a)

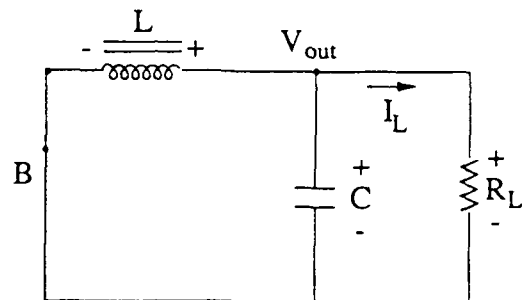


(b)

Figure 3.5: Buck DC-DC Converter Model: (a) Basic Circuit Topology, (b) Utilization of a BJT and a Freewheeling Diode, D_1 , as a Switch



(a)



(b)

Figure 3.6: Resulting Topological Changes in the Buck DC-DC Converter due to the Positioning of the Switch: (a) Switch-On, (b) Switch-Off

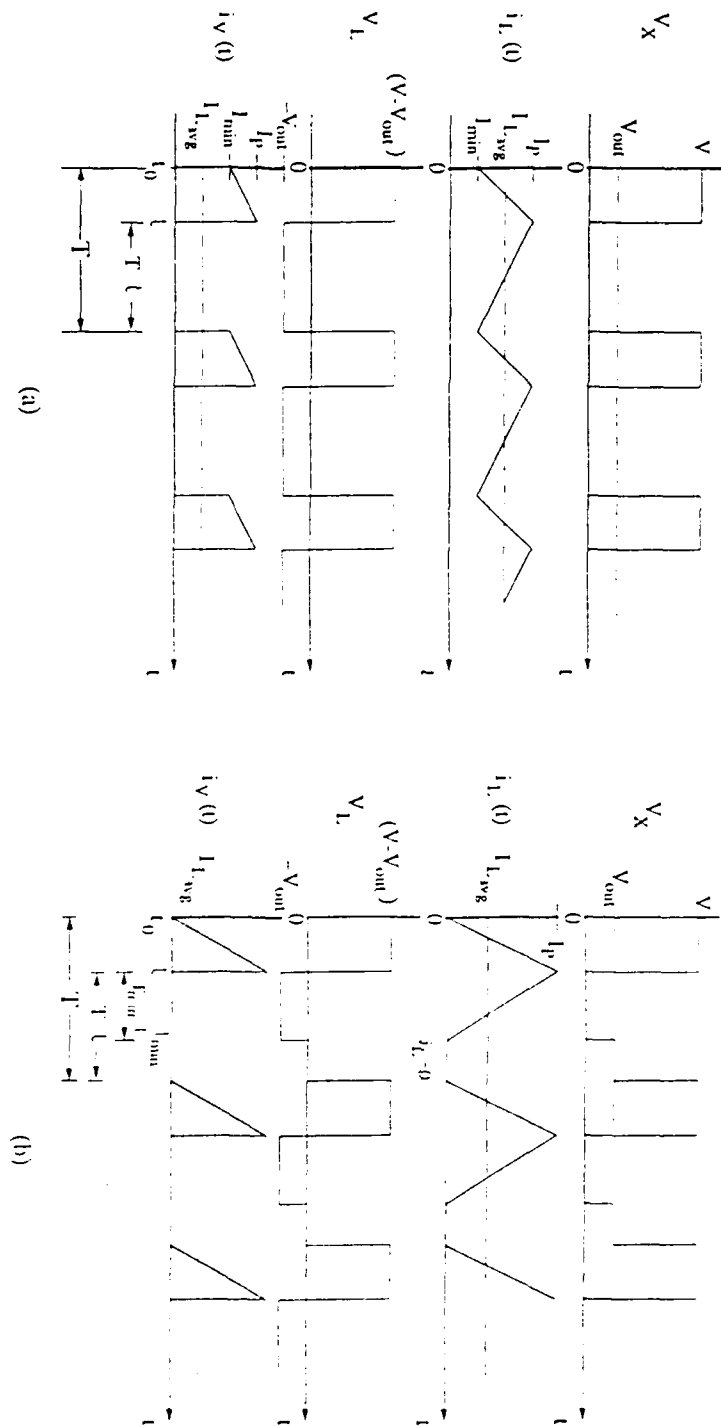


Figure 3.7: Buck DC-DC Converter Switching Waveforms: (a) Continuous Conduction Mode, (b) Discontinuous Conduction Mode [After Ref. 16]

the inductor must be equivalent. Therefore, it can be stated that over two switched intervals,

$$\int_0^{DT} V_L dt = - \int_{DT}^T V_L dt \quad (3.3)$$

$$\text{Energy stored [volt - sec]} = \text{Energy released [volt - sec]}$$

or after completing the necessary integral calculation noted above:

$$(V - V_{out})DT = V_{out}(1 - D)T \quad (3.4)$$

As a result of this criterion, a Buck dc-dc converter functioning in the continuous conduction mode will have a duty cycle, D , of,

$$D = \frac{V_{out}}{V} \quad (3.5)$$

By defining M , a commonly used dimensionless parameter, as the dc voltage ratio (or converter gain) as

$$M \triangleq \frac{V_{out}}{V} \quad (3.6)$$

the step-down dc conversion ratio for a Buck dc-dc converter can be expressed as.

$$M = D \text{ [Continuous conduction mode]} \quad (3.7)$$

Equating Equation 3.2 to 3.5, it is obvious that V_{out} will always be less than V in value.

In the discontinuous conduction mode, the energy stored in the inductor during the interval, τ , and then subsequently recovered during discharge. $\tau_{min} - \tau$, or D_2T , is slightly different than the aforementioned case or,

$$(V - V_{out})DT = V_{out}(T_{min} - \tau)T \quad (3.8)$$

where T_{min} is the period of maximum switching frequency.

This equation, which reduces to

$$V_{out} = \frac{VD}{D + (T_{min} - \tau)} = \frac{VD}{D + D_2} , \quad (3.9)$$

allows for a step-down conversion ratio of

$$M = \frac{V_{out}}{V} = \frac{D}{D + D_2} \text{ [Discontinuous conduction mode]}. \quad (3.10)$$

To develop a similar relationship for the dc voltage conversion ratio of a Buck converter functioning in its discontinuous mode, it first must be understood that the dc output current ($I_{L_{AVG}} = \frac{V_{out}}{R_L}$) found in the load must match the average value of the current present in the inductor over time T or, from Figure 3.7b,

$$I_{L_{AVG}}T = \frac{I_p\tau}{2} + \frac{I_p}{2}(T_{min} - \tau) . \quad (3.11)$$

Peak current, I_p , in the inductor can easily be determined from the very well-known inductor voltage relationship

$$V = L \frac{di}{dt} \quad (3.12)$$

as being

$$I_p = \tau \frac{(V - V_{out})}{L} = DT \frac{(V - V_{out})}{L} \text{ (For inductor charge)} \quad (3.13)$$

and, equivalently,

$$I_p = V_{out} \frac{T_{min} - \tau}{L} = V_{out} \frac{D_2T}{L} \text{ (For inductor discharge)}. \quad (3.14)$$

Therefore, by substitution of Equation 3.13 into Equation 3.11, Equation 3.15 results,

$$I_{L_{AVG}} = \frac{V_{out}}{R_L} = \frac{V_{out}D_2T}{2L} [D + D_2] \quad (3.15)$$

in order to achieve an equation for D_2 . The equation for D_2 is

$$D_2(D, K) = \frac{-D \pm \sqrt{D^2 + 4K}}{2} = \frac{K}{D} \frac{2}{1 + \sqrt{1 + \frac{4K}{D^2}}} \quad (3.16)$$

where

$$K = \frac{2L}{R_L T} = \frac{2Lf_s}{R_L} \quad (3.17)$$

This produces the desired result of

$$M(D, K) = \frac{V_{out}}{V} = \frac{2}{1 + \sqrt{1 + \frac{4K}{D^2}}} \quad [\text{Discontinuous conduction mode}] \quad (3.18)$$

in terms of D and K by careful substitution of Equation 3.16 into Equation 3.10 for D_2 .

It is very important to note the dramatic effect the parameters D_2 , D , and K have on the voltage out of a Buck dc-dc converter operating in the discontinuous conduction mode. The dc gain exhibits a very strong dependence on switching frequency, inductor size, loading condition and duty cycle. This outcome is in very sharp contrast with Equation 3.7, the result for the continuous conduction mode.

A converter can be operated in an open or closed loop manner.

In an open-loop consideration, the converter is operated independently of the feedback regulator [Ref. 18:p. 148]. The duty cycle, D , is given and externally controlled (independently generated) [Ref. 19:pp. 117-118]. Consequently, the decay ratio, D_2 , is a function of K and D as found in Equation 3.16.

In a closed-loop consideration, the dc output voltage is kept constant regardless of the input voltage by maintaining control over the duty cycle (PWM) or T_{min} (FM). The type of regulator used for PWM control adjusts the value of D , and hence D_2 is strictly dependent upon D and K . It therefore becomes accommodating to develop an expression for D and D_2 in terms of M and K . Equations 3.16 and 3.18 can be rearranged to create

$$D(M, K) = \sqrt{\frac{KM^2}{1-M}} \quad (3.19)$$

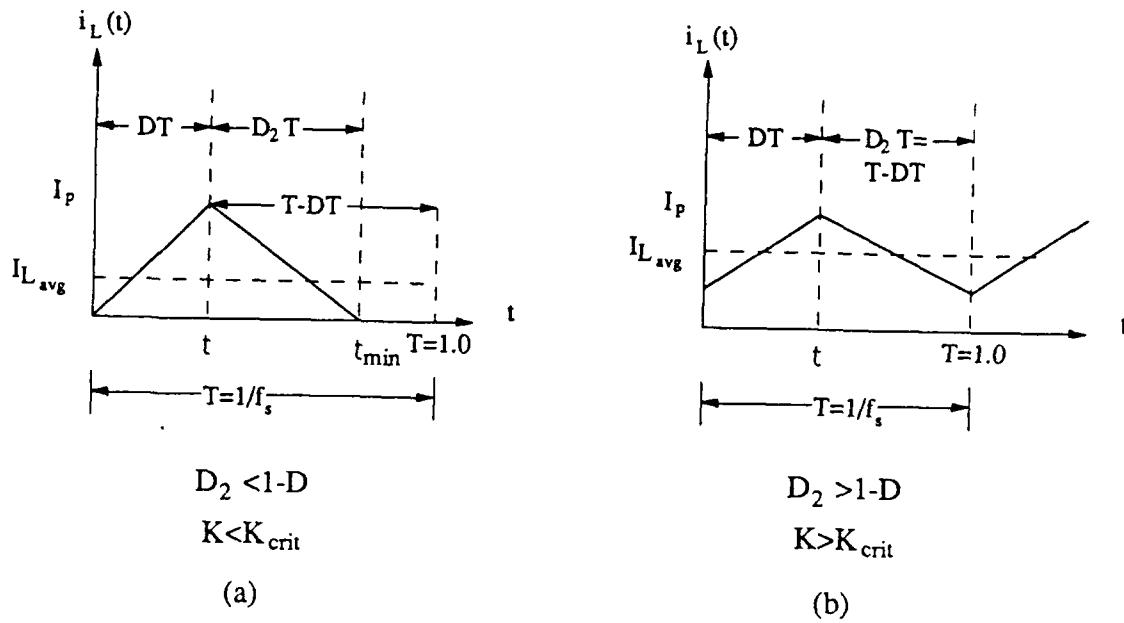


Figure 3.8: Inductor Current Conduction Mode Boundary Relationship:
 (a) Discontinuous Conduction Mode, (b) Continuous Conduction Mode
 [After Ref. 16]

and

$$D_2(M, K) = \sqrt{K(1 - M)} \quad (3.20)$$

[Ref. 18:pp. 148-149, Ref. 19:p. 116]

(3) Boundary Condition Determination

It is now important to investigate the condition which determines whether a dc-dc converter is operating in the continuous or discontinuous mode. The boundary that splits the two modes apart is solely dependent upon the size of the inductor current decay interval. Using Figure 3.8 as a sample waveform, this principle is illustrated as follows.

When interval D_2T is less than interval, $T - \tau$, or equivalently, $T(1 - D)$, the converter operates in the discontinuous conduction mode. Thus,

$$D_2 < 1 - D \text{ [Discontinuous conduction mode]}. \quad (3.21)$$

If, though, D_2 , the decay ratio, is made greater than the switch-off ratio, then the switch-mode converter will function in the continuous conduction mode yielding to the condition:

$$D_2 > 1 - D \text{ [Continuous conduction mode]}. \quad (3.22)$$

It is important to notice, again, how inductor current in each case varies within the interval, T . The guideline established for the boundary between two conduction modes in the case of the Buck converter therefore becomes:

$$D_2 = 1 - D \text{ [Ref. 19 : p. 117]}. \quad (3.23)$$

The critical value of K , $K_{critical}$, as defined in Equation 3.17, which defines the boundary between two conduction modes can be determined by placing D_2 from Equation 3.16 into Equation 3.23 to form:

$$K_{crit} = 1 - D . \quad (3.24)$$

As a result, the criteria for defining the correct operating mode for any dc-dc converter becomes

$$K \triangleq K_{crit} \text{ Limiting case between conduction modes ,} \quad (3.25)$$

$$K < K_{crit} \text{ Discontinuous conduction mode , and} \quad (3.26)$$

$$K > K_{crit} \text{ Continuous conduction mode .} \quad (3.27)$$

[Ref. 18:p. 149, Ref. 19:p. 117, 125]

By plotting Equation 3.24 in Figure 3.9, the range of operation for a Buck dc-dc converter can clearly be determined. If K is greater than $K_{crit}(D)$, as specified by the operating parameters L , R , and f_s , then the switch-mode converter will always function in the continuous conduction mode, independent of duty cycle D . However, when K is less than K_{max} , the switch-mode converter operates in the discontinuous conduction mode. $K_{crit,max}$ is the maximum value of D possible for the function given in Equation 3.24.

Equation 3.24 defines $K_{crit}(D)$ for the open loop consideration. For the closed loop case, when it is more suitable to describe the boundary condition in terms of the dc gain, M , the parameter D can be proven equal to M by substitution of Equation 3.23 into Equation 3.10 for D_2 and reducing the result. The criterion for K_{crit} is thus established by replacing D with M in Equation 3.24 to form:

$$K_{crit}(M) = 1 - M \quad (3.28)$$

Graphing D vs. $M(D, K)$ (Equation 3.18) in both conduction modes provides interesting insight into the dc voltage gain characteristics of the Buck dc-dc converter. It is evident from Figure 3.10 that transition from one conduction mode into another for the Buck dc-dc converter occurs at higher values of D when $K \ll 1$. In the continuous conduction mode, M behaves in a highly linear fashion in contrast to its opposing mode of operation. A Buck dc-dc converter functioning in its discontinuous conduction mode increases in its degree of non-linearity in inverse proportion to K .

Transition from a continuous to a discontinuous mode of operation for a Buck dc-dc converter with a maximum K_{crit} value of less than one can be achieved by varying the duty cycle, D , as just shown in Figure 3.9 and Figure 3.10. The range of the duty cycle, D , or its corresponding gain, $M(M = \frac{V_{out}}{V})$, is

important when designing a closed loop system in which the output voltage V_{out} is held constant over a widely varying range of input voltages, V .

From an operational viewpoint, the design engineer usually is most interested in how a change of load, R_L , will affect the converter operating mode. As load resistance, R_L , is increased to a high R value and the average inductor current is reduced below some critical value R_{crit} , a converter will enter into its discontinuous mode of operation. Figure 3.11 indicates the effect load has on the inductor current waveform as load resistance, R_L , is increased. Diode, D_1 , in Figure 3.5, acting as an unidirectional current element, prevents waveform C from occurring. Inductor current is unable to reverse its direction of flow during switch off-time. Further decrease in load current beyond the limit set by R_{crit} causes inductor current to remain at zero. By defining R_{nom} as

$$R_{nom} \triangleq 2Lf_s = \frac{2L}{T} \quad (3.29)$$

K can be described in terms of R_L to obtain:

$$K = \frac{2L}{R_L T} = \frac{R_{nom}}{R_L} \quad (3.30)$$

Now, another criterion for determining the boundary separating two conduction modes of operation can be established using

$$R = R_{crit} \quad (3.31)$$

to produce

$$R_L > R_{crit} \text{ [Discontinuous conduction mode]} \quad (3.32)$$

and

$$R_L < R_{crit} \text{ [Continuous conduction mode]}. \quad (3.33)$$

[Ref. 14:p. 288, Ref. 15:p. 149, Ref. 19:p. 118, 125]

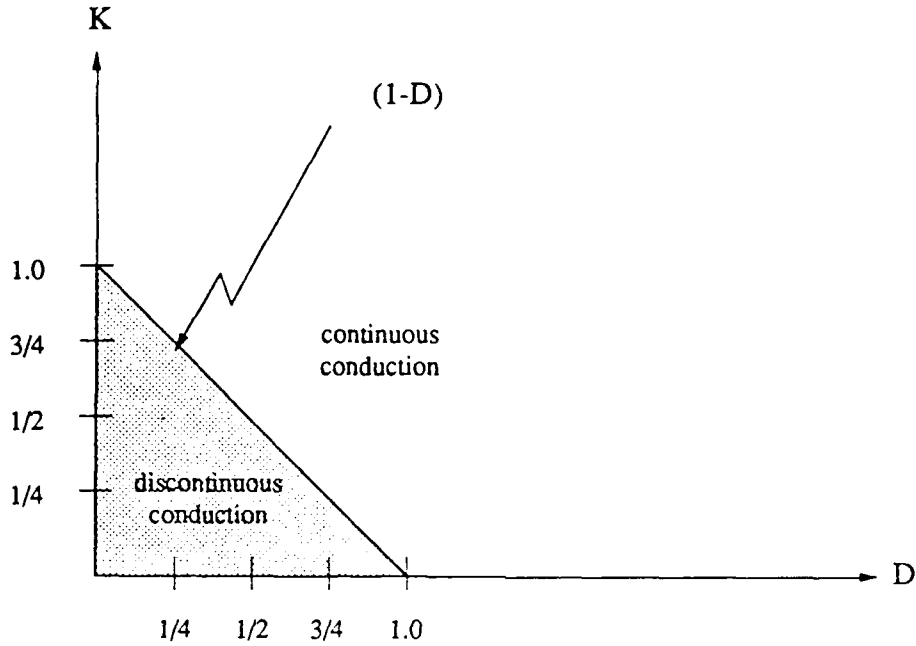


Figure 3.9: Determination of Conduction Mode Boundary Analyzing K vs. $K_{crit}(D)$ [After Ref. 16, 19]

The preceding two equations can be best expressed as being the dual relationships to Equations 3.26 and 3.27 respectively. By replacing K in Equation 3.30 with K_{crit} from Equation 3.24 and solving for R , an expression for R_{crit} can be found for the open loop consideration as being:

$$R_{crit}(D, R_{nom}) \approx \frac{R_{nom}}{1-D} . \quad (3.34)$$

Similarly, an equation for R_{crit} in the closed loop condition can be developed using Equations 3.28 and 3.30 to yield

$$R_{crit}(M, R_{nom}) \approx \frac{R_{nom}}{1-M} . \quad (3.35)$$

Table 3.1 and Figure 3.12 are included to summarize the conditions and vividly illustrate how the parameters load of resistance, R_L , inductance, L , switching frequency, f_s , and duty cycle, D , affect the boundary condition of a

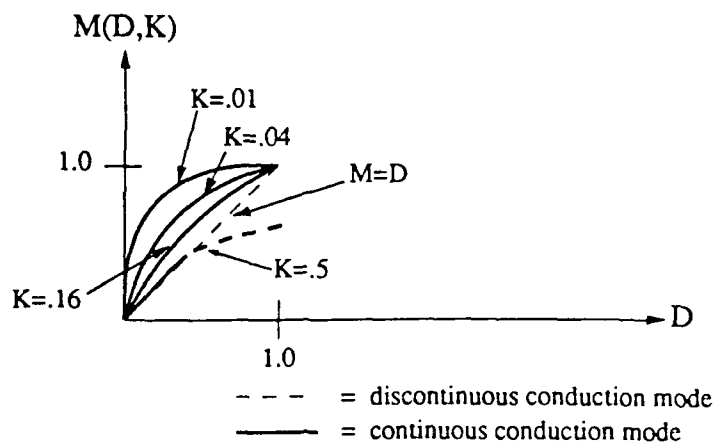


Figure 3.10: DC Voltage Gain Characteristic for the Buck DC-DC Power Converter [After Ref. 16]

Buck dc-dc converter. A qualitative increase in load resistance R_L , and for a decrease of L , f_s , and/or D will cause a switch-mode converter to transition into its discontinuous conduction mode of operation.

2. Resonant Converters

Resonant converters have been used in a wide variety of applications requiring high power density. The development of this circuit has evolved due to the inability of the square-wave converter to handle switching losses. The resonant converter when compared to a traditional Buck PWM converter offers the following advantages:

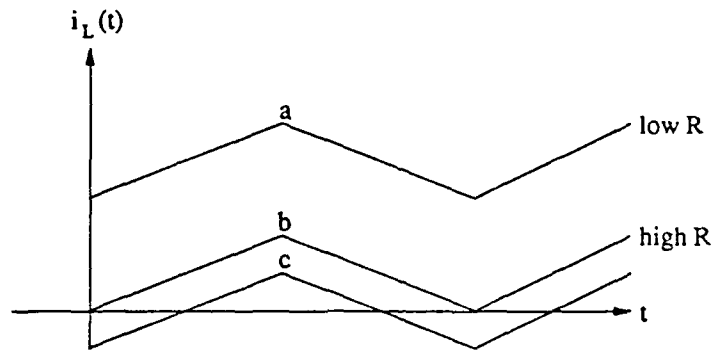


Figure 3.11: Inductor Current Conduction Mode Boundary Relationship as a Function of Load Resistance [After Ref. 14]

TABLE 3.1: Boundary Conditions Between Two Conduction Modes

CONTINUOUS CONDUCTION MODE		DISCONTINUOUS
$R < R_{crit}$		$R > R_{crit}$
$K > K_{crit}$	$K < \frac{2L}{RT}$	$K < K_{crit}$
$D_2 > 1 - D$		$D_2 < 1 - D$
$M = D$		$M = \frac{D}{D + D_2}$

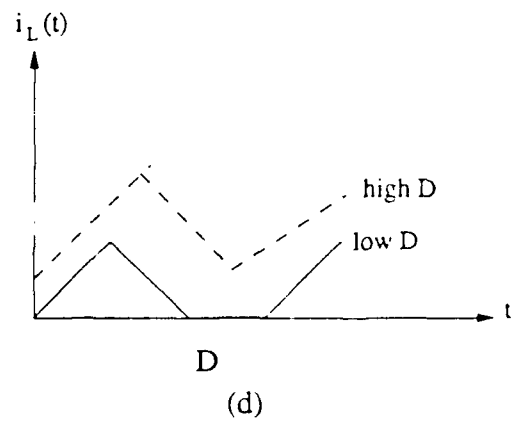
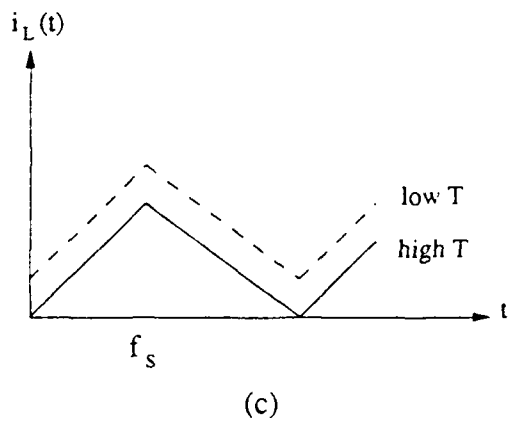
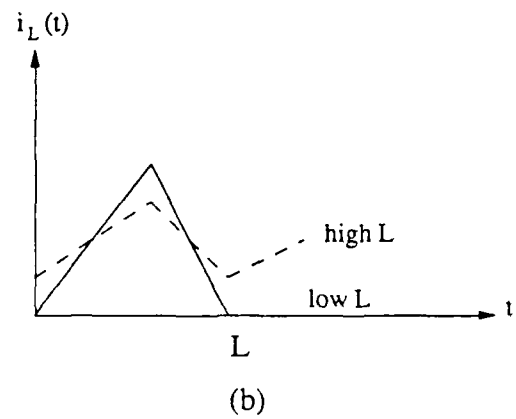
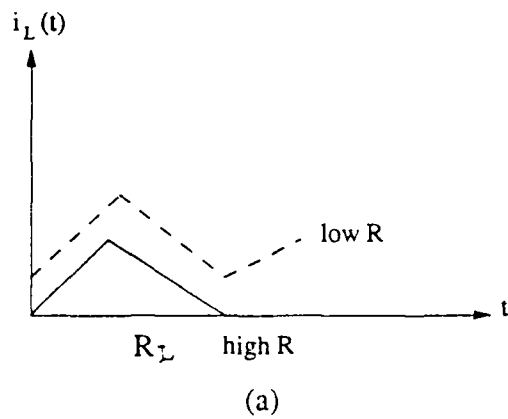


Figure 3.12: Parameters Affecting the Boundary Conditions of the Buck DC-DC Power Converter: a) Resistance, b) Inductance, c) Switching frequency, d) Duty Cycle [After Ref. 14]

- Higher efficiency due to reduced switching losses,
- Smaller weight and volume in magnetic elements, filter components, and heat sink,
- Reduced EMI from zero current switching, and
- Increased reliability from reduced switching stresses.

The resonant technique processes power in a sinusoidal fashion. Resonant converters use L-C tank circuits, which can be repetitively excited by a power source through the gating of semiconductor switches. Energy is exchanged back and forth with a time constant that is a function of the L-C product. This action is attained at times of zero current by opening and closing switching elements in series with the resonant current. Turn-off under zero-current conditions reduces switching stresses and switching losses. [Ref. 9:pp. 4-6, Ref. 20:p. 365, Ref. 21:p. 221]

The two most popular resonant converters in use today are the Series Resonant Converter (SRC) and the Parallel Resonant Converter (PRC), shown in Figure 3.13 [Ref. 22:p. 545, Ref. 23:p. 232]. A PRC obtains its power by tapping the tank's capacitor, while a SRC must tap its inductor current to acquire energy. [Ref. 12:p. 222]

Figure 3.14 shows a simple resonant converter using switches to produce a square-wave voltage across a series LRC network. The current that flows is approximately sinusoidal and in phase with the square-wave voltage at resonance. As the frequency at which the circuit operates is moved further away from the point of resonance, the tank impedance rises, reducing load current and power. Excessive

deviation from resonance produces a phase difference between load current, I_L , and square-wave voltage, V_{sw} . [Ref. 5:p. 367]

Resonant technology, although frequently used in high power SCR motor drives and uninterrupted power supplies, has not gained wide acceptance in low voltage dc-dc converter applications. Due to circuit complexity and phase differences occurring in resonant converters under certain conditions, quasi-resonant converters have become the popular alternative. They too share the main advantage of resonant converters, that is, the semiconductor switch can be naturally commutated using sinusoidal current waveforms produced by an L-C tank circuit. [Ref. 5:pp. 366-377, Ref. 21:p. 7, Ref. 11:p. 377]

3. Quasi-Resonant Buck DC-DC Converter

a. Circuit Element Topology

Figure 3.15 illustrates a quasi-resonant Buck dc-dc converter in its half-wave mode configuration. This type of circuit represents a whole new generation of converters. The quasi-resonant converter is a descendant of both the PWM converter and resonant converter. Consequently, this new converter topology benefits from having a resonant tank circuit that produces a pseudo-sinusoidal current or voltage waveform in the resonant switch and a continuous resonant inductor current or resonant capacitor voltage waveform that is not broken up by intermittent operation of the transistor power switch. [Ref. 21:pp. 7-8]

Like a true series resonant converter, a quasi-resonant converter is preferred to PWM regulation in applications concerning high power and high switching frequencies. Use of either a zero-current switching or zero-voltage switching technique permits operation primarily at a higher switching frequency while reducing switching loss, lowering device stress, and cutting size of reactive energy-storage elements [Ref. 25:p. 472]. This important discovery comes at a time when use of

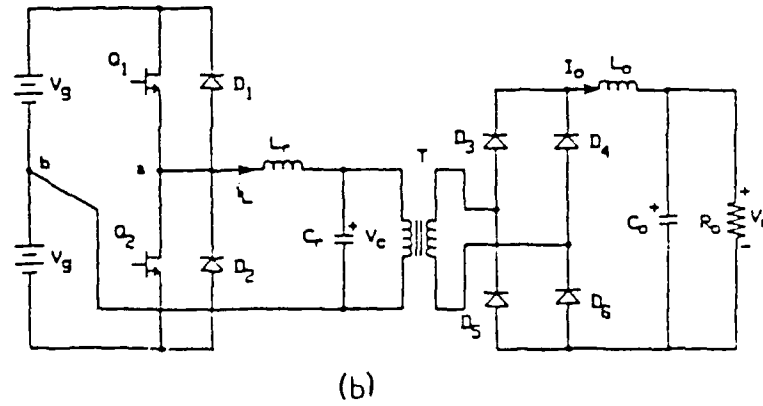
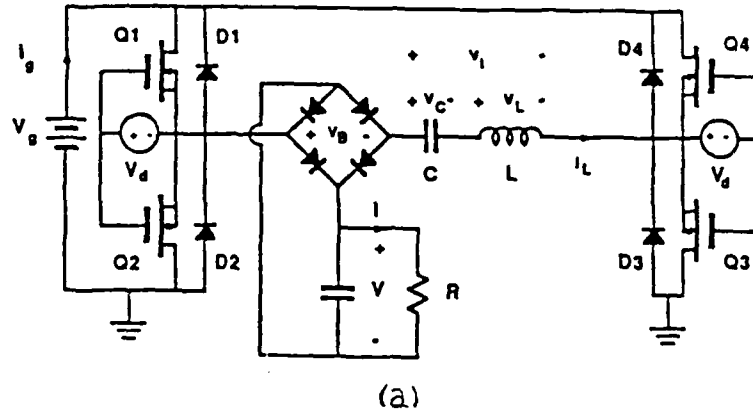


Figure 3.13: (a) Full Bridge Series Resonant Converter, (b) Half Bridge Parallel Resonant Converter [From Ref. 22, 23]

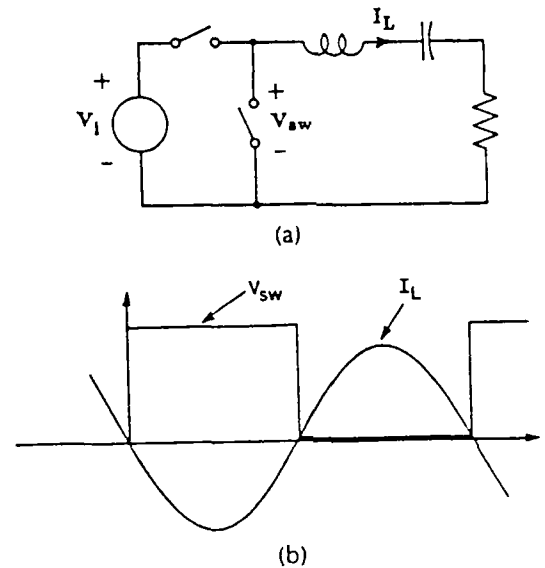


Figure 3.14: a) A Voltage Source, Series Resonant Converter, b) Switch Waveforms Showing Zero Current Transitions [From Ref. 5]

new power MOSFETs at switching speeds of tens of megahertz (MHz) is imminent. However, capacitive turn-on loss has restricted operation of this type of converter to a switching frequency of 1-2 MHz; conduction loss is generally greater since the sinusoidal current gives rise to increased rms current [Ref. 11:p. 377, Ref. 25:p. 55].

A quasi-resonant converter is formed by inserting a resonant switch into the proper location of a conventional PWM controlled Buck dc-dc converter. A resonant switch is comprised of the following components: a resonant inductor, L_r , a resonant capacitor, C_r , and a semiconductor switching device [Ref. 21:p. 278, Ref. 24:p. 472, Ref. 26:p. 107, Ref. 27:p. 395]. As viewed in Figure 3.16, the resonant inductance, L_r , is always placed in series with the switch to moderate the change in current with respect to time, and a resonant capacitor is added as an additional energy storage and transfer element [Ref. 21:pp. 11-12, Ref. 24:p. 472].

The series resonant, L-type, switch topology is employed in Figure 3.15. It is used when current-waveform shaping is desired. Note, also, the placement

of resonant capacitor, C_r ; it is connected in parallel to the series combination of the switch and resonant inductance, L_r . The L-C tank circuit is necessary to cause current resonance in the circuit as energy is periodically interchanged between the resonant inductor and capacitor. This is done to ensure that the transistor can be naturally commutated on and off at zero-current, instead of being forced off by an applied gate signal. [Ref. 21:p. 12, Ref. 28:p. 381-382]

Positioning of diode D_2 (in Figure 3.15) is important when determining actual flow of switch current and switch mode type of operation. As shown, diode D_2 will only allow the switch current to resonate in its positive half cycle and operate in a half-wave mode. However, a full-wave configuration is easily obtained by placing diode D_2 anti-parallel to the switching device, giving the switch current a bidirectional flow. Figure 3.16 illustrates the resonant switch characteristics of both half-wave and full-wave configurations for each L and M type of switch. [Ref. 11:p. 378, Ref. 21:p. 12, Ref. 26:p. 107]

Application of the resonant switch is not limited to just the Buck converter, but has found use in all variations of the basic Boost, Buck-Boost, Cuk, and their derivatives as well. Figure 3.17 gives a graphical comparison of these quasi-resonant topologies vs. their standard PWM converter counterparts. [Ref. 21:p.23, Ref. 24:p. 476]

b. Circuit Analysis of the Quasi-Resonant Buck DC-DC Converter

In order to develop useful expressions for voltage and current relationships which accurately describe the behavior of the ZCS, quasi-resonant dc-dc converter, the following assumptions are essential:

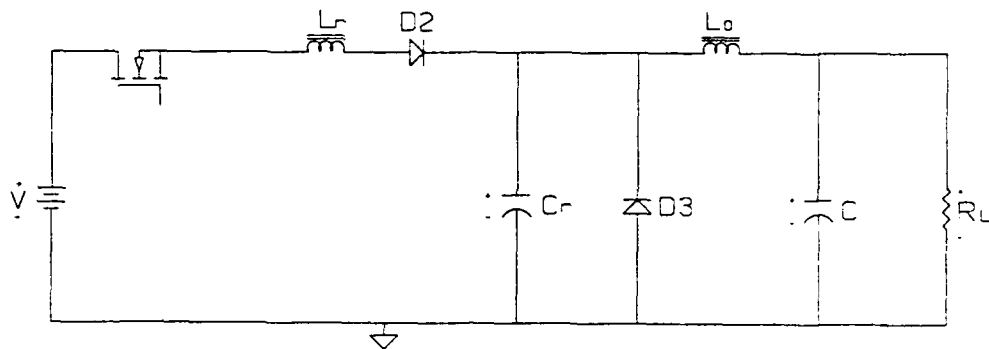
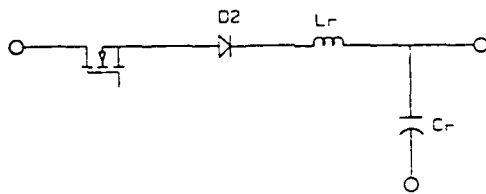
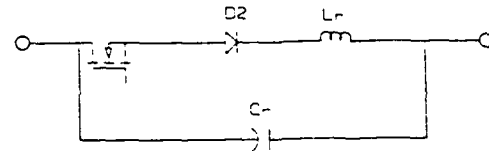


Figure 3.15: Quasi-Resonant Buck DC-DC Converter

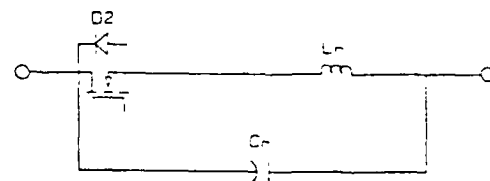
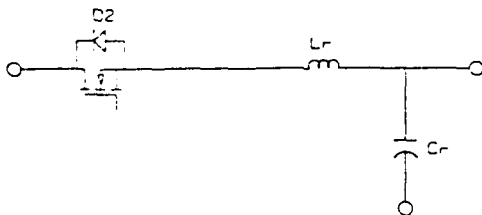
L-Type



M-Type



(a)



(b)

Figure 3.16: Current-mode Resonant Switch Topology: (a) Half-wave Mode, (b) Full-wave Mode [From Ref. 21]

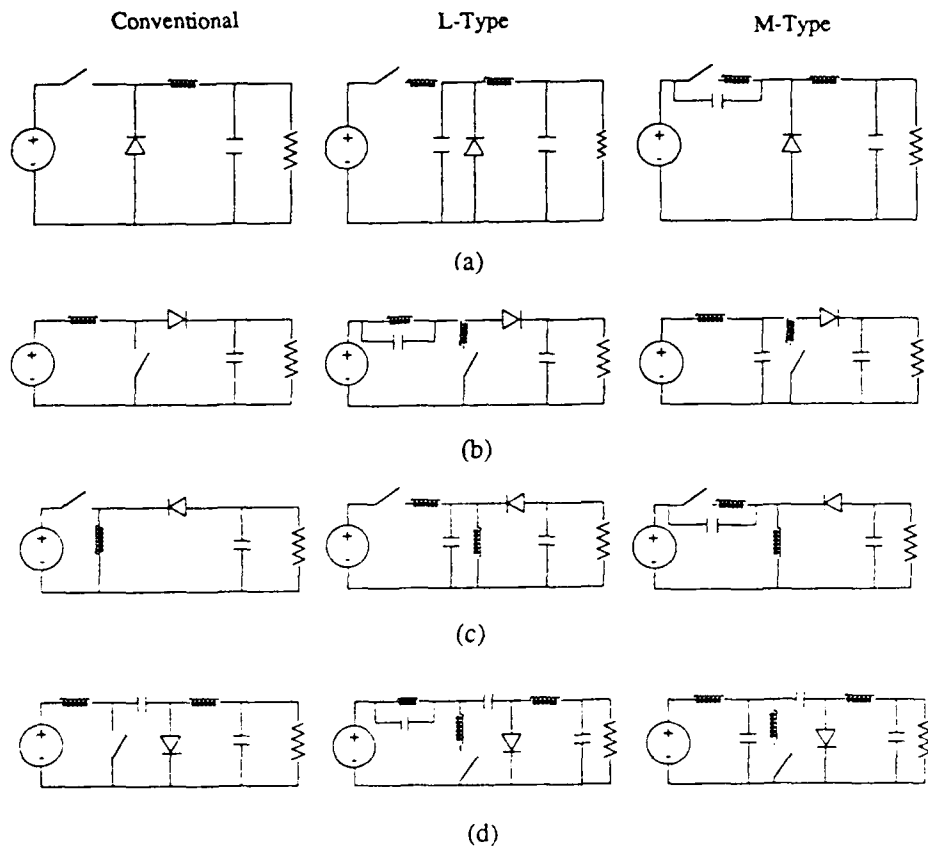


Figure 3.17: Zero-Current Switched Quasi-resonant Converters: a) Buck, b) Boost, c) Buck-Boost, d) CUK [After Ref. 21, 24]

- All semiconductor devices used are ideal, implying zero saturation voltage from negligible on resistance, zero leakage current in the off-state because of infinite off resistance, zero switching loss due to zero current rise and fall times, and zero capacitance.
- Switch diode, D_2 , and free wheeling diode, D_3 , are ideal.
- All reactive elements are lossless, linear, passive, and time invariant in behavior without any parasitic elements.
- L_0 is chosen to be much larger than L_r to ensure L_0-C resonates at a frequency greater than $L_r - C_r$ [Ref. 29:p. 345].
- The output filter, $L_0 - C$, and load resistance, R_L , are modeled as a constant current sink given that inductance and capacitance of the filter are large enough to produce a constant current and voltage output. [Ref. 11:p. 380, Ref. 21:p. 15, Ref. 26:p. 344, Ref. 30:p. 287]

(1) Mode I: Resonant-Freewheeling State

A ZCS, quasi-resonant Buck dc-dc converter having two primary switches, sw and D_3 , can be characterized by its four distinct modes of operation as shown in Figure 3.18. The analysis begins prior to time $t = 0$ with the switch, sw , being open and the capacitor voltage, V_{Cr} , set at zero volts. Current provided by current sink, I_L , flows through forward-biased diode, D_3 , in a closed loop fashion during this first mode.

(2) Mode II: Inductor-Charging State

At time $t = 0$, the switch is closed and Mode II begins. Current flow through forward-biased half-wave diode, D_2 , charges inductor, L_r , at a rate of

$$\frac{dI_{L_r}}{dt} = \frac{V - V_{Cr}}{L_r} = \frac{V}{L_r} \quad (3.36)$$

where

- V = input voltage, and
- I_{L_r} = resonant inductor current.

Current generated by the inductor is not allowed to charge the resonant capacitor, as a result of changing the bias on diode D_2 , until the instantaneous resonant inductor current, $I_{L_r}(t)$, exceeds the output current, I_L . The voltage V_{Cr} thus remains clamped at zero volts until time, T_1 , as pictured in Figure 3.19. The duration of Mode II is, from Equation 3.36

$$T_{10} = \frac{I_L L_r}{V} . \quad (3.37)$$

(3) Mode III: Resonant-Charging State

Mode III marks the beginning of the resonant charging state in the quasi-resonant converter as diode D_3 is commutated off. During this interval $[T_1, T_3]$, the current waveforms of the resonant capacitor and the resonant inductor are quasi-sinusoids. The period of time to resonantly charge the resonant capacitor voltage, V_{Cr} , from 0 to $2V$ with a current of

$$I_{Cr}(t) = I_{L_r}(t) - I_L \quad (3.38)$$

requires

$$T_{21} = \pi \sqrt{L_r C_r} \quad (3.39)$$

which is equal to one-half of the resonant circuit period.

Both the resonant inductor, L_r , and the resonant capacitor, C_r , are constrained in size by the relationship governing resonant frequency. This condition expressed as a function of L_r and C_r is defined as:

$$f_r = \frac{1}{2\pi \sqrt{L_r C_r}} . \quad (3.40)$$

In a current-mode resonant switch, the periodic interchange of energy between resonant components L_r and C_r takes place mainly during switch on-time. Resonant inductor current is dependent upon the energy shared between the resonant elements L_r and C_r . Therefore, peak current passing through a power semiconductor device used in a ZCS, quasi-resonant converter is always greater than its corresponding PWM converter counter-part [Ref. 21:p. 66, Ref. 28:p. 384]. Resonant inductor current, I_{L_r} , reaches its maximum value,

$$I_{L_{rmax}} = \frac{V}{\sqrt{\frac{L_r}{C_r}}} \quad (3.41)$$

at time $T_1 + \Delta t$, when capacitor resonant voltage, V_{C_r} , equals input voltage, V .

Equations describing the behavior of current flowing through inductor, I_{L_r} , and voltage present in resonant capacitor, V_{C_r} , are found by applying Kirchoff's Laws. First, the voltage drop across inductor, L_r , from T_1 to T_3 is

$$V - V_{C_r}(t) = L_r \left(\frac{dI_{L_r}}{dt} \right) \quad (3.42)$$

The current through the capacitor, C_r , which is proportional to the instantaneous time rate of change of voltage, can be determined using Equation 3.38 and rewritten as

$$I_{L_r}(t) - I_L = C_r \left(\frac{dV_{C_r}}{dt} \right) \quad (3.43)$$

Realizing that $I = \frac{dQ}{dt}$, Equation 3.42 can be written in operator form as

$$\left(D^2 + \frac{1}{C_r L_r} \right) Q = \frac{V}{L_r} \quad (3.44)$$

where

- $D = \frac{d}{dt}$, and
- Q = instantaneous charge present in the resonant capacitor.

Equation 3.44 is solved as a second-order linear differential equation in terms of Q . Knowing that $V_{C_r}(0) = 0$, the result,

$$V_{C_r}(t) = \frac{Q}{C_r} = V(1 - \cos \omega t) \quad (3.45)$$

is obtained for the voltage present in the resonant capacitor from T_1 to T_3 . This then allows an expression for the current through the resonant inductor, I_{L_r} , to be formed as a function of its alternating current (ac) and dc components. This is accomplished by replacing V_{C_r} in Equation 3.43 with Equation 3.45 and solving to yield

$$I_{L_r}(t) = \sqrt{\frac{C_r}{L_r}} (V \sin \omega t) + I_L \quad (3.46)$$

Close examination of this current waveform in Figure 3.19 requires that the ac component of resonant inductor current always be greater than its corresponding dc component. If, for a given input voltage, V , the load current, I_L , is ever greater than the magnitude of its corresponding ac component of resonant inductor current, then the zero-current property will be forfeited. The current, $I_{L_r}(t)$, because of its size, will be unable to decrease to zero due to the proportion of I_L . [Ref. 11:p. 383]

During this third mode of operation, a second point in time exists when $I_{C_r}(t)$ in Equation 3.38 once again equals zero. This occurs at time T_2 in Figure 3.19 when V_{C_r} is equivalent to $2V$. The time for the resonant current to completely ring down from $I_L(T_2)$ to zero at switch turn-off $I_L(T_3)$ is directly related to

$$I_L = I_{L_r} \sin \left[2\pi \frac{T_{32}}{T} \right] = I_{L_r} \sin \left[\frac{T_{32}}{\sqrt{L_r C_r}} \right] \quad (3.47)$$

The duration of this particular segment lasts approximately

$$T_{32} = \left(\frac{1}{\omega} \right) \left[\sin^{-1} \left(\frac{I_L}{I_{L_r}} \right) \right] = \left(\frac{1}{\omega} \right) \left[\sin^{-1} \left(I_L \frac{Z}{V} \right) \right] \quad (3.48)$$

where

- $w = \frac{1}{\sqrt{L_r C_r}}$, and
- $Z = \sqrt{\frac{L_r}{C_r}}$ (Resonant characteristic impedance).

(4) Mode IV Resonant Capacitor-Discharge State

Time T_3 is used to mark the beginning of Mode IV as indicated in Figure 3.18(e) and 3.19. Switch sw is naturally commutated off as instantaneous resonant inductor current, $I_{L_r}(t)$, falls to zero. Prompted by a reverse voltage of $V_{C_r} - V$, diode D_2 is used to prevent any reverse current flow through the resonant switch.

During time interval T_{43} , the resonant capacitor's voltage discharge to the load is linear as voltage V_{C_r} drops. The rate at which this energy exchange takes place is proportional to the load current, i.e.,

$$\frac{V_3}{T_{43}} = -\frac{I_L}{C_r} \quad (3.49)$$

where V_3 is the voltage at time T_3 .

To determine the time it takes the circuit to complete this action requires an expression for V_3 . Knowing that the voltage is in a state of decay dictates use of a negative cosine function to properly describe its waveform. Therefore,

$$V_3 = V + V \cos [\omega T_{32}] \quad (3.50)$$

or after further computation V_3 expressed in terms of V , I_L , and Z becomes:

$$V_3 = V + \sqrt{V^2 - (I_L Z)^2} \quad (3.51)$$

Finding the time interval over which this process quickly occurs now becomes a simple matter of substituting Equation 3.51 for V_3 of Equation 3.49.

Thus,

$$T_{43} = \frac{C_r V}{I_L} \sqrt{\left[1 + \left(1 - \left(I_L \frac{Z}{V}\right)\right)\right]} . \quad (3.52)$$

Equation 3.52 describes the ability of the resonant capacitor, C_r , to discharge energy in a given period of time. In a ZCS, quasi-resonant converter, resonant cycles of fixed on-time, T_0 to T_3 , or T_{30} , are separated by non-resonant stages of variable off-time, T_3 to T_5 , or T_{53} . Control of the circuit's resonant capacitor, C_r , as shown in Figure 3.19, is very important in regulation of switching frequency and transfer of power.

(5) Mode I - Revisited

The next mode is a repetition of the first. From time T_4 to T_5 , or T_{54} , current originating from the current sink, I_L , flows through the freewheeling diode, D_3 . As pictured in Figure 3.19, until the next voltage (V_{GS}) is applied and inductor charging begins, inductor current will remain at zero.

The total period of the quasi-resonant Buck dc-dc converter switching cycle is denoted by T , and is defined as the sum of all combined time intervals, or

$$T = T_{10} + T_{21} + T_{32} + T_{43} + T_{54} . \quad (3.53)$$

Overall, Equations 3.45 and 3.46 determine the maximum current and voltage ratings required from a zero-current quasi-resonant Buck switching element. Maximum permissible peak resonant current through the switch is

$$I_{su_{max}} = V \sqrt{\frac{C_r}{L_r}} + I_L . \quad (3.54)$$

The maximum forward voltage possible that can be delivered to the switch is V . The above mentioned fixed resonant parameters C_r and L_r are again important, since their magnitude controls switching frequency and peak resonant of the waveform directly.

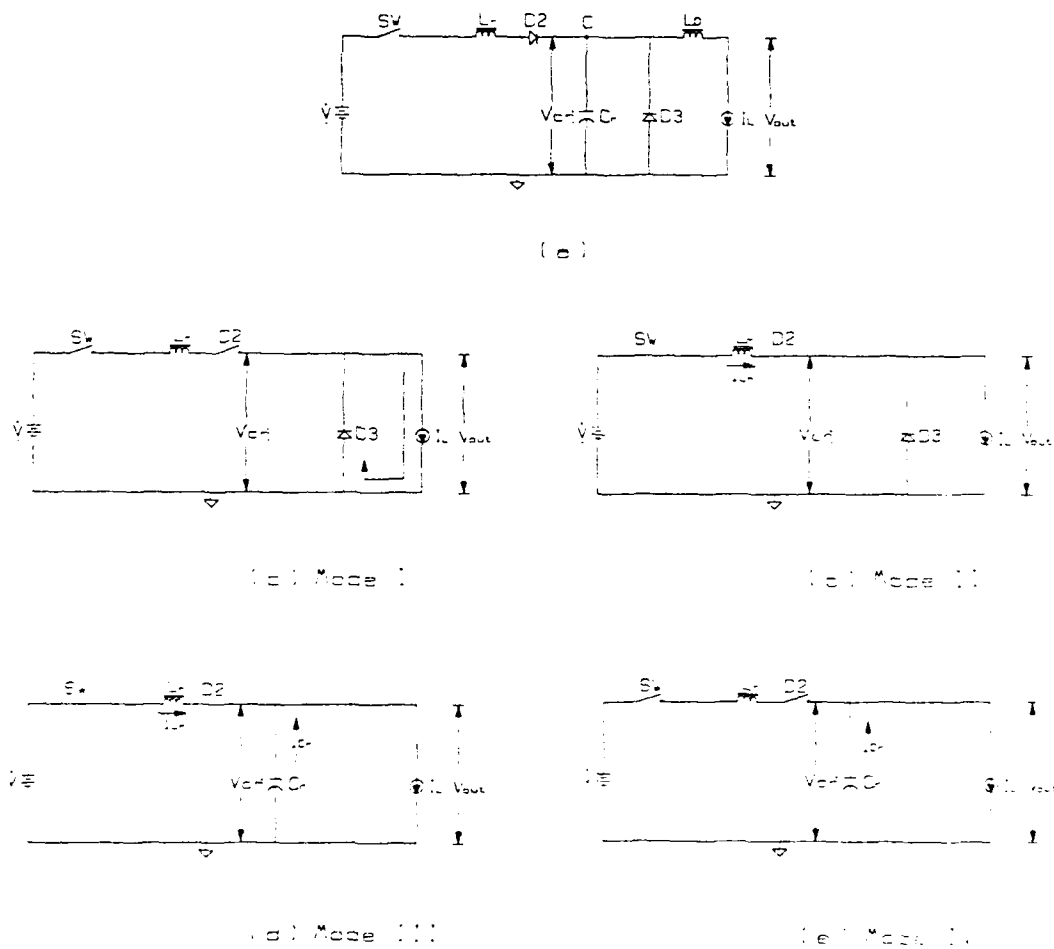


Figure 3.18: Various Modes of a ZCS, Quasi-Resonant Buck DC-DC Converter

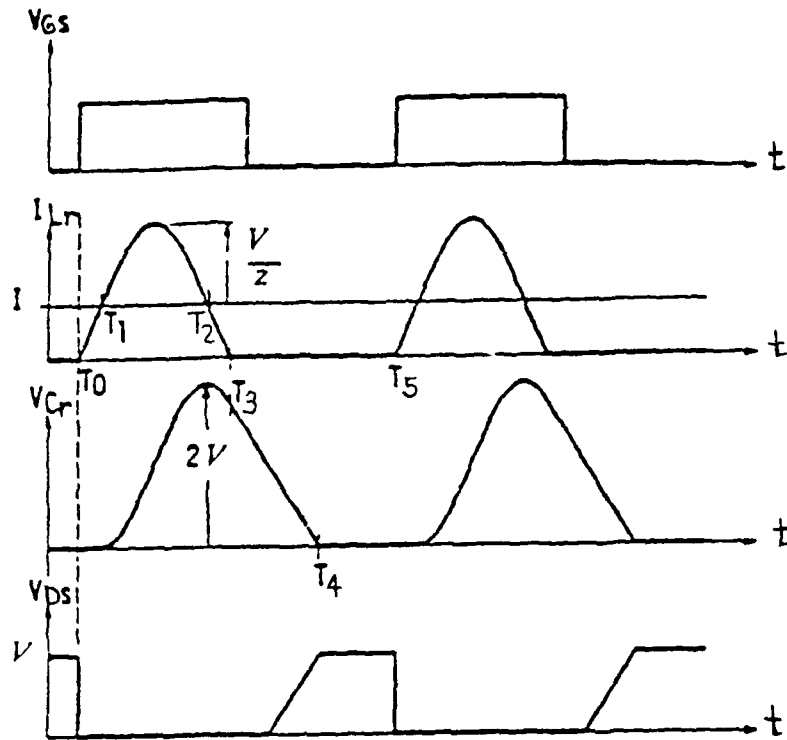


Figure 3.19: Half-wave Mode Waveforms of a ZCS, Quasi-Resonant Buck DC-DC Converter [After Ref. 21]

c. DC Voltage Conversion Ratio

Once again, M , a dimensionless parameter, is used to describe the dc conversion ratio or dc gain of the quasi-resonant dc-dc converter as being:

$$M = \frac{V_L}{V} \quad (3.55)$$

The input energy stored in resonant inductor, L_r , during the switch turn on time, $T_{30} = T_3 - T_1$, must equal the energy released per cycle to the load. Therefore, equating the input energy, E_i , to the output energy, E_o , produces

$$V \int_{T_0}^{T_1} I_{Lr}(t) dt + V \int_{T_1}^{T_2} I_{Lr}(t) dt + V \int_{T_2}^{T_3} I_{Lr}(t) dt = I_L V_L T \quad (3.56)$$

$$\text{Energy stored [volt - sec]} = \text{Energy released [volt - sec]}.$$

To greatly simplify matters, manipulation of Equation 3.56 can be made less strenuous if the quasi-resonant current waveform is considered to be a near perfect sinusoid. Equation 4.19 then can be written as

$$V I_{in_{avg}} = V_L I_L \quad (3.57)$$

where $I_{in_{avg}}$ is the average resonant input current viewed by the switch.

This now permits use of the approximation described in Equation A-1.2 to determine the average resonant input current as seen by the switch. Thus, the dc conversion ratio expressed as a function of average input and output current becomes

$$M = \left[\frac{I_{in_{avg}}}{I_L} \right] = \frac{2}{\pi} \left[\frac{T_{30} I_{su_{max}} L_r}{T_{10}} \right] \quad (3.58)$$

It can also be shown, after several calculations, that the output voltage in Equation 3.56 is equal to

$$V_{out} = \frac{V}{T} \left[\left(\frac{1}{2} \right) T_{10} + T_{31} + T_{43} \right] \quad (3.59)$$

[Ref. 29:p.348]

Research by several authors has exposed the sensitivity of the dc voltage conversion ratio for the quasi-resonant Buck converter to load variation. As shown in Figure 3.20, the voltage conversion ratio for the half-wave mode is very sensitive to different loading conditions in comparison to the full-wave mode. Under a heavy current loading condition, the majority of the energy generated by the resonant L-C rank circuit is delivered and consumed by the load. However, under a light load condition, when R_L is large, resonant inductor current, $I_{Lr}(t)$, becomes less. This fact is understandable, since $V_L = I_L R_L$ and time interval ΔT_{10} must decrease for a constant output voltage. Consequently, $I_{Lr}(t)$ in Equation 3.46 will have a smaller constant dc value, I_L , and, in comparison to a heavy load condition, will oscillate less in the first half of the resonant cycle and have a lower overall negative value in its second half cycle. Hence, a quasi-resonant switch in the quasi-resonant Buck converter, operating in a full-wave condition, can compensate for a varying load by passing more or less reverse current through the anti-parallel diode. But a Buck resonant converter built to function in the half-wave mode must resort to a frequency alteration to regulate its output voltage. Therefore, under very heavy load conditions, dc voltage gain for a quasi-resonant Buck converter operating in either mode, can be shown to equal,

$$M = \frac{V_{out}}{V} = \frac{f_s}{f_n} \quad (3.60)$$

where is the circuit resonant frequency.

If duty cycle, $\left(\frac{\tau}{T}\right)$, is substituted for frequency, this result is identical to that of a PWM Buck converter. Notice, also, that the dc voltage conversion ratio, as defined by Equation 3.60, is completely independent of load resistance. [Ref. 11:pp. 383-383, Ref. 21:pp. 26-27, Ref. 26:pp. 110-111, Ref. 29:pp. 348-349]

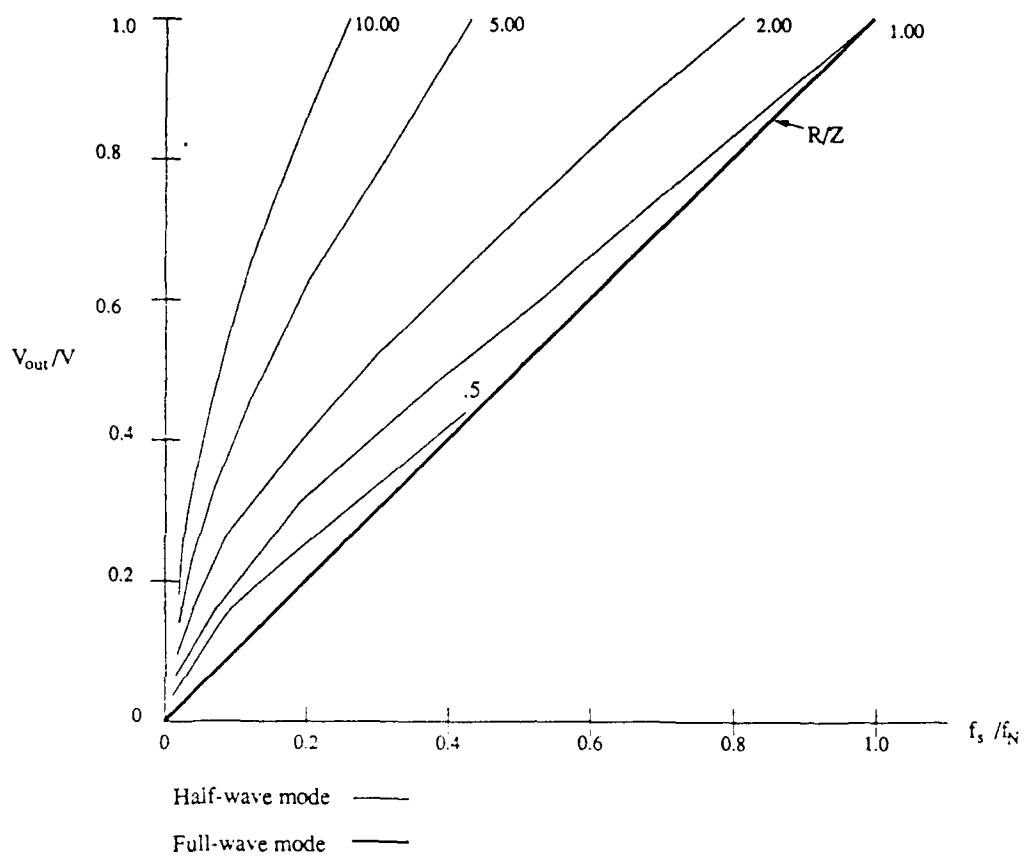


Figure 3.20: DC Voltage Conversion Ratio for the ZCS, Quasi-Resonant Buck Converter [After Ref. 26]

IV. SWITCHING ELEMENT SELECTION

The arrival of fast power switching solid state devices of the bipolar, MOSFET, and thyristor variety has brought about a revelation of change in the techniques used in development of new smaller dc-dc power converters. Each type of semiconductor device has its own individual strengths and weaknesses. The research in this thesis supports the use of a power MOSFET over a minority carrier device, due to its superior performance. This section is used to identify and discuss key power MOSFET electrical characteristics highlighted in Table 4.1. A comparison is made between a BJT and the enhancement mode (N-channel) power MOSFET. Subsequent paragraphs are used to discuss certain device power losses and salient operating characteristics which factor into current waveform waveshaping.

A. MOSFETS MATURE

The transistor, when used as a switch and forced to operate under harsh conditions, is probably the most highly stressed component in a dc-dc power converter circuit. A poor switch design will place severe limitations on system efficiency and reliability. Hence, higher frequencies have mandated the use of transistors as switching elements in converter designs today.

In the beginning, BJTs were preferred over MOSFETs as switching elements. MOSFETs found no application in the switch-mode power converter industry due to rating limitations and relatively high conduction losses. As shown in Figure 4.1, development of power MOSFET technology started to increase dramatically in the latter part of the 1970's when the fabrication process used in their manufacture was modified. Improvements in device on-resistance per unit area, particularly in the

TABLE 4.1: Power MOSFET Electrical Characteristics

	DEVICE		
	BJT [NPN]	PARAMETER	MOSFET [N CHANNEL]
A	Middle (20 ~ 80 kHz)	Switching Frequency	Very High (100 kHz ~ 2 MHz)
P	Middle	Cost	High
P	Middle (500 V)	Voltage	High (1200 V)
R	Middle ($10^1 \sim 10^2$)	Current Gain	High ($10^5 \sim 10^8$)
A	Middle (150 °C)	Maximum Operating Temp	High (200 °C)
I	Low ($10^3 \sim 10^5 \Omega$)	Input Impedance	Very High ($10^9 \sim 10^{11} \Omega$)
S	Low	On Resistance	High (60 ~ 250 milli Ω for 100 V)
A	High	Off Resistance	High ($10^9 \Omega$)
L	Good	Ruggedness	Excellent
R	Limited at Higher Frequencies	SAO	Exceptionally Stable
A	Minority	Semi-conductor type	Majority
T	Current	Device Control Type	Voltage
I	Elaborate	Control Circuitry	Simple
N	Yes	Second Breakdown	No
G	Negative	Temperature Coefficient	Positive

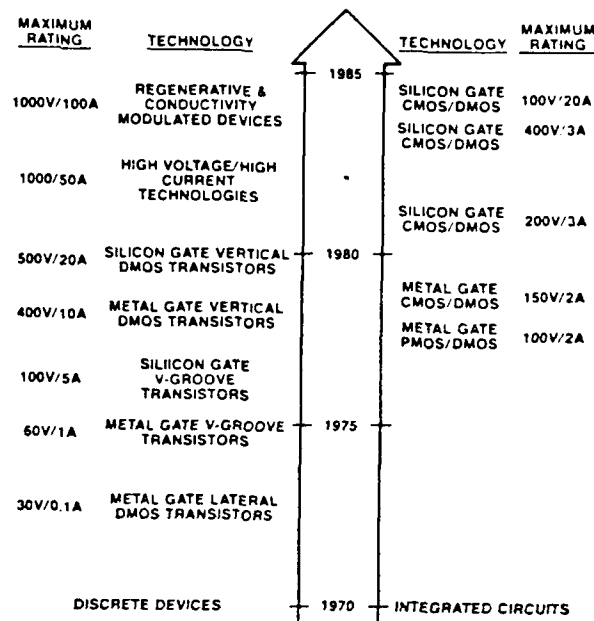


Figure 4.1: Milestones in the Growth of Power MOS Technology [From Ref. 31]

low voltage region coupled with their high breakdown voltage, low current leakage, ruggedness, and ease of use have made MOSFETs an attractive alternative in the power electronics industry. [Ref. 31:p. 448, Ref. 32:pp. 311, 418]

Double-diffused or DMOS technology, as shown in Figure 4.2, has replaced conventional surface-groove technology, called VMOS. This MOS structure eliminates many of the voltage and on-resistance limitations of conventional MOS transistors by maintaining a tight tolerance over channel-length reproducibility to within 1 to 2 mm and by heavily doping the body region (p-doped area) in comparison to the N drain (epitaxy) region during each diffusion cycle. [Ref. 9:p. 2.20, Ref. 33:p. 216, Ref. 34:p. 23]

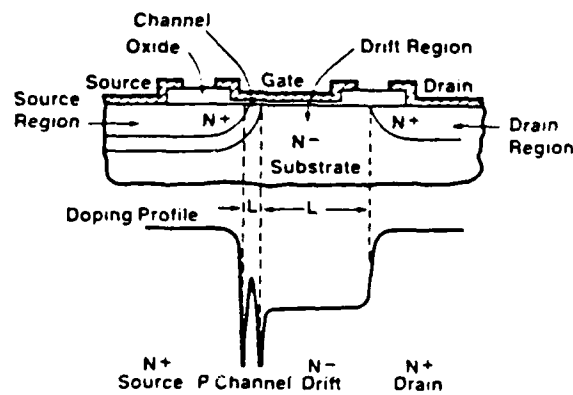


Figure 4.2: The Structure and Dopant Profile of a Lateral DMOS Field Effect Transistor [From Ref. 33]

The development of the power MOSFET has evolved due to the need of a switching device that can operate well above the 20 kHz frequency plane [Ref. 35, p. 90]. The appeal of the MOSFET comes mainly from its switching behavior. Unlike a BJT, a MOSFET is a majority-carrier device capable of ultra high switching speeds, as indicated in Figure 4.3. The speed at which either device switches is proportional to time delays within its structure and the presence of different capacitances which must be alternately charged and discharged. The MOSFET's high operating frequency allows for unexpected power density, and reduced output noise and ripple. [Ref. 33:p. 217, Ref. 37:p. 13, Ref. 38:p. 16, Ref. 39:p. 91]

B. DEVICE TURN-ON CHARACTERISTICS

In a BJT, movement of carriers is from the emitter to collector region through the base. Electrons which are injected from the emitter to the base are labelled minority carriers. For a BJT, turn-on requires only that the capacitances associated with the junction be charged. However, when switched off, poor turn-off behavior

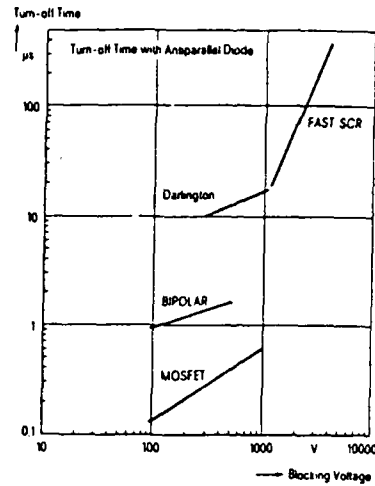


Figure 4.3: Turn-off Time as a Function of Rated Blocking Voltage for MOSFETs, Bipolar Power Transistors and Fast Switching SCRs [From Ref. 36]

is observed for this minority carrier device. Upon application of reverse base drive current, the stored charge in the semiconductor material required to sustain current flow results in a storage time that reduces its turn-off speed. [Ref. 33:p. 217]

The MOSFET, on the other hand, is a voltage-controlled device. A MOSFET is turned on by applying a voltage within specified limits between the gate and source to produce a current flow in the drain. Current flow from source to drain is supported by majority carriers.

C. EFFECT OF INTERNAL CAPACITANCES

A MOSFET is capacitive in nature. Figure 4.4 provides a cross-sectional view of a power MOSFET and its associated capacitances. During each switching cycle when the MOSFET is turned on, the MOSFET's parasitic input capacitance, C_{iss} , must be charged and then discharged to make the channel conductive. This tiny input capacitance used to model the metal-oxide gate structure itself is formed as

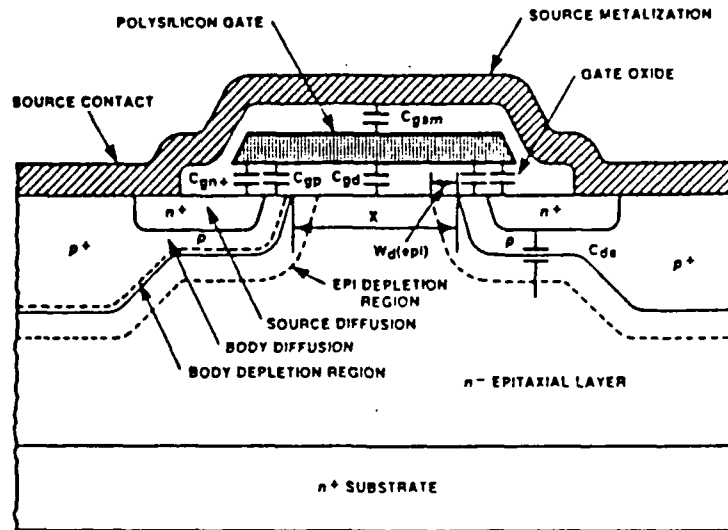


Figure 4.4: Cross Sectional View of a VDMOS Power FET Showing the Origin of the Interelectrode Capacitances [From Ref. 9]

a result of several manufacturing limitations and design trade-offs. It is defined as being

$$C_{iss} = C_{GS} + C_{GD} \quad (4.1)$$

where

- C_{GS} = Gate-to-source capacitance, and
- C_{GD} = Gate-to-drain capacitance. [Ref. 31:p. 92, Ref. 32:p. 312, Ref. 34:p. 24, Ref. 35:p. 91]

A MOSFET reacts as a resistive device and dissipates additional energy as the gate drive is used to charge C_{iss} past a threshold voltage. To attain higher switching speeds, the source impedance of the driving voltage source is kept low. Ultimately, the speed at which this device switches is dependent upon the ability of the gate driving source to supply and remove gate charge. Therefore, the total average rate

drive dissipation, P_G , within a power MOSFET is equal to,

$$P_G = C_{iss} V_{GS}^2 f_s \left[\frac{R_G}{(R_G + R_{DR})} \right] \quad (4.2)$$

or

$$P_G = Q_G V_{GS} f_s \left[\frac{R_G}{(R_G + R_{DR})} \right] \quad (4.3)$$

where

- C_{iss} = MOSFET input capacitance,
- V_{GS} = Peak gate-to-source input voltage equal to $(V_{on}^2 + V_{off}^2)$,
- f_s = Switching frequency,
- Q_G = Peak gate charge,
- R_G = Internal gate resistance,
- R_{DR} = External drive resistance. [Ref. 9:p. 4-6, Ref. 38:p. 17, Ref. 39:p. 96, Ref. 40:p. 407]

Although, input capacitance in reality is non-linear in nature; for simplicity, it is approximated as a constant value. [Ref. 33:p. 217, Ref. 35:p. 91, Ref. 37:p. 13, Ref. 41:p. 151]

In today's MOSFETs, the above loss becomes significant only at very high switching frequencies in the megahertz range. Not only does this capacitance increase switching time, but, its energy is lost twice each cycle. Power dissipated in the gate drive circuit can be diminished by use of a resonant technique to charge C_{iss} . If the differential voltage $(V_{on} - V_{off})$ is used to increase switching speed, it is accomplished at the expense of a substantial power loss. [Ref. 5:p. 365-366, Ref. 11:pp. 386-387, Ref. 40:p. 408]

Another loss that must be considered is the power loss related to the MOSFET's output capacitance, C_{oss} . This parameter, which is defined as

$$C_{oss} = C_{DS} + C_{DG} , \quad (4.4)$$

where

- C_{DS} = Drain-to-source capacitance, and
- C_{DG} = Drain-to-gate capacitance,

contributes greatly to switch loss in a Buck square-wave dc-dc converter, especially when V_{DS} is greater than 100 volts [Ref. 4:p. 62, Ref. 9:p. 3-6]. This loss,

$$P_{sw-on} = \frac{1}{2} f_s C_{oss} V_{DS}^2 \quad (4.5)$$

where V_{DS} is the drain-to-source voltage prior to turn-on is not affected by how fast the channel can turn on. This is because, at device turn-off, the MOSFET channel becomes very high in impedance, forcing the commuting load current to charge the output capacitance. Energy entering into the MOSFET during this time interval is stored within C_{oss} until its voltage, V_{DS} , equals the voltage in V . There is no energy dissipation until the MOSFET is turned on again to complete the switching transition. At this point, energy is lost as load current commutates to the free wheeling diode, causing C_{oss} to discharge through the drain. [Ref. 4:pp. 62-63, Ref. 40:p. 404]

At switching frequencies above 1 MHz range, the energy contained within C_{oss} must be conserved to preserve efficiency [Ref. 6:p. 58, Ref. 11:p. 378]. Two options exist. First, a MOSFET can be constructed with a lower value of C_{oss} . But, usually with this kind of change comes an increase in on-resistance, $R_{DS(on)}$, and conduction loss. A more favorable result is obtainable if a zero-voltage switching technique is

used to shape transistor voltage and achieve zero-voltage at turn-on. [Ref. 4:pp. 62-63, Ref. 21:pp. 3-4, Ref. 40:p. 404]

D. DEVICE TURN-OFF AND OFF-RESISTANCE

Turn-off circuitry for a power MOSFET conversely is very simple in comparison to that of a BJT. Removal of the gate-to-source voltage instantly causes the channel between source and drain to become high in impedance (10^9 ohms) [Ref. 34:p. 23]. Having a layer of SiO_2 between the gate and body electrically isolates all current flow from the applied voltage source into the gate, except for minor leakage currents (I_{DSS} – microamperes). This characteristic allows power MOSFETs to be driven directly by CMOS or TTL circuitry. On account of this, power loss, P_L , due to drain-to-source leakage,

$$P_L = I_{DSS}V_{DS}(1 - D) \quad (4.6)$$

is usually disregarded unless T_j (junction temperature) is high or V_{GS} is not significantly less than the threshold voltage of the device during switch off-time [Ref. 9:p. 4.7]. [Ref. 35:pp. 91-92, Ref. 37:p. 13]

A power MOSFET, because it is not limited by minority charge storage effects, has a very short turn-off time as previously demonstrated in Figure 4.3. Switching time is a direct function of gate capacitance and available drive current. Turn-off capability of a minority carrier device, e.g., a BJT, can be improved by using added external circuitry, but its performance is degraded by one or more of the following inadequacies:

- Greater circuit complexity,
- More frequent voltage and current spikes,
- Increased switching loss, and/or

- Greater limitations on circuit switching frequency and/or load range. [Ref. 21:pp. 2-3]

Hence, power MOSFETs are better suited devices for use in low power, high frequency applications. [Ref. 9:p. 4.7, Ref. 33:p. 217, Ref. 39:p. 91]

E. STATIC OPERATING CHARACTERISTICS

A MOSFET, when utilized as a switch, cycles from time to time from its saturation region to its cutoff region and vice versa. Comparison of typical output characteristic curves for both the MOSFET and BJT devices shows the MOSFET in Figure 4.5 having a constant resistance (ohmic region) and constant current (saturation) region. When turned on and V_{DS} is small, the MOSFET will operate in the linear region of the curve where drain current, I_D , is proportional to drain-to-source voltage, V_{DS} . Application of additional drain-to-source voltage causes the device to move past pinch-off into a region of constant drain current. It is the actual increase in drain current which compels carriers to move through the channel area, causing a transverse voltage drop to occur. This in turn creates an increase in on-resistance as the channel shortens. For values of V_{DS} greater than ten volts, the MOSFET behaves as a current source if V_{GS} is held constant. Transition from one state to another is strictly gate-to-source voltage dependent. The relationship of on-resistance as a function of gate voltage and channel current is illustrated in Figure 4.6, [Ref. 9:p. 5.72]. [Ref. 9: pp. 2.2, 5.71, Ref. 34:p. 24, Ref. 38:p. 93-94]

F. ON-RESISTANCE

A MOSFET, as previously stated, when in its constant resistance region, functions as a resistor. Figure 4.7 reveals each of the internal parasitic resistances found in this device. In a power MOSFET, most loss suffered comes from on-resistance,

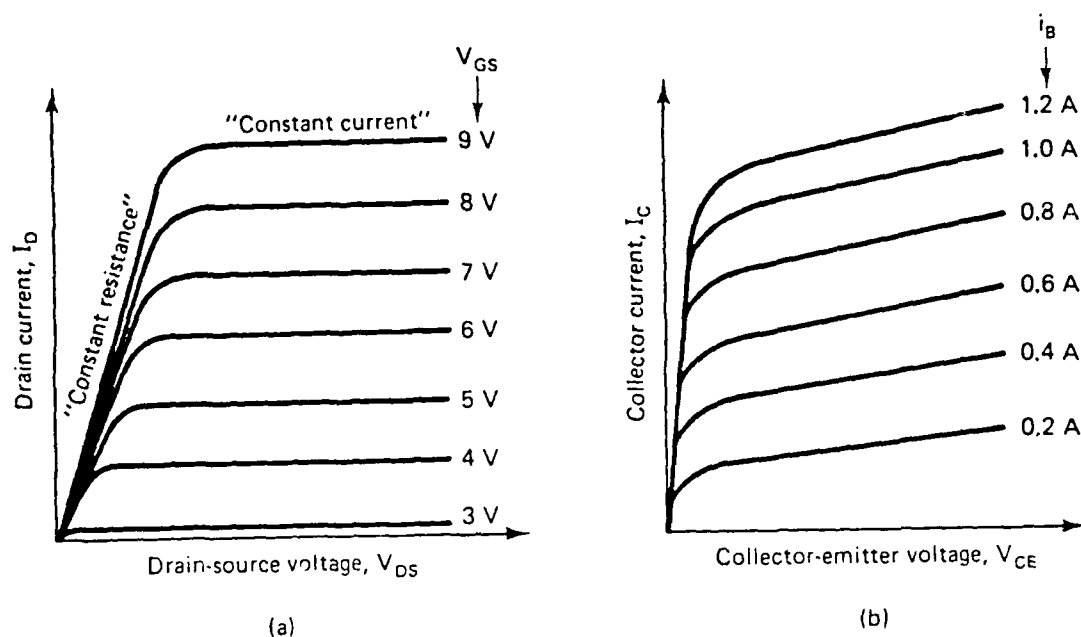


Figure 4.5: Comparison of Idealized Output Characteristics of a) Power MOSFET, b) Bipolar Power Transistor [From Ref. 34]

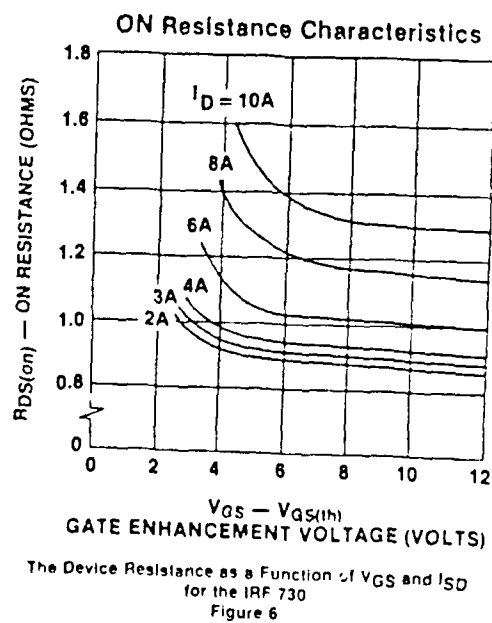


Figure 4.6: Device Resistance as a Function of V_{GS} and I_D [From Ref. 9]

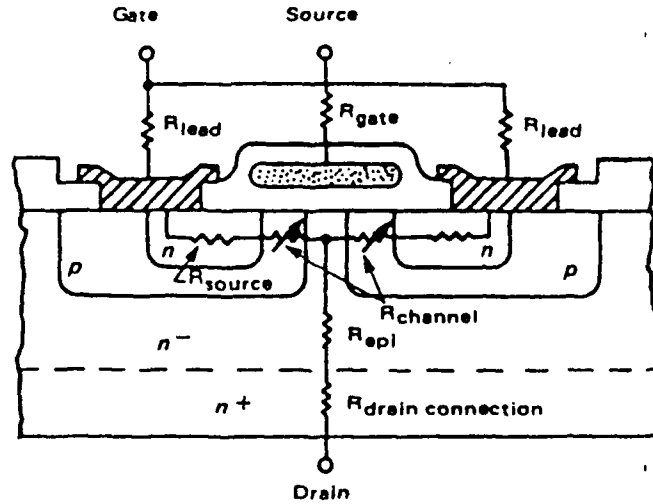


Figure 4.7: MOSFET Internal Parasitic Resistances [From Ref. 9]

$R_{DS(on)}$, through which all drain-to-source current, I_D , must flow. The on-resistance of a power MOSFET is very important because it determines conduction voltage drop, power handling capacity, and an efficiency of a device [Ref. 42:p. 212].

Conduction loss, as previously defined in Equation 2.3, is once again stated as

$$P_{cond} = f_s \tau I_D^2(rms) R_{DS(on)} \quad (4.7)$$

Conduction losses are not a function of $R_{DS(on)}$ and I_D alone, but are dependent upon junction temperature, T_J , gate-to-source voltage and manufacturing variations [Ref. 9:p. 4.7].

Characteristic of all MOSFETs, each has a positive temperature coefficient as shown by the BUZ-60 specification sheet located in Appendix C. As a rule, $R_{DS(on)}$ will double approximately for every 110°C rise in junction temperature. Power dissipation will increase as well, but switch time will remain a constant. A BJT, on the other hand, is less stable thermally. Its switching loss is increased with temperature, usually doubling every 100°C. [Ref. 41:p. 152]

In general, for the same die size and junction temperature, on-resistance will grow for a given voltage rating, due to the device's internal resistance distribution [Ref. 9:p. 4.8]. For example, a BUZ 347 rated at 50 V possesses a value of 0.03 Ω in comparison to a BUZ 311 rated at 1000 V, which typically has a value of approximately 6 Ω . Also, channel resistance, $R_{channel}$, which is determined by the channel length, gate oxide thickness, carrier mobility, threshold voltage, and actual gate voltage applied to the device is more dominating in low voltage devices. Epitaxial layer thickness and resistivity, R_{epi} , are more important in high voltage applications in conjunction with higher drain-to-source voltage rating requirements, as illustrated in Figure 4.8. Epitaxial layer thickness selection is crucial in minimizing device on-resistance for a given breakdown specification and die size [Ref. 9:p. 2.51].

Conduction losses for a BJT, as defined by,

$$P_{cond} = \frac{\tau}{T}(i_c V_{ce} + i_{be} V_{be}) \quad (4.8)$$

where

- τ = Switching element on-time,
- T = Switching period,
- i_c = On-state collector current,
- V_{ce} = On-state collector-to-emitter voltage,
- i_{be} = Base-to-emitter current, and
- V_{be} = Base-to-emitter voltage.

are usually considered minimal in a switch-mode power converter. The design engineer has the option of selecting an optimum base current, i_b , that will force the

transistor into saturation, lessen power dissipation as a result of V_{ce} , and prevent losses due to high current in the drive circuitry. The ability to bias a BJT and limit conduction loss results in a significant advantage in voltage drop for a given current over a power MOSFET. However, a trade-off exists since switching performance is degraded for each increase in base current, i_b , due to a growth in storage time. This handicap retards device efficiency in regard to switching frequency. [Ref. 33:p. 217, Ref. 43:pp. 396-397, Ref. 44:p. 200]

At switching frequencies below 1 MHz, on-state conduction loss is much more severe in a MOSFET than a BJT [Ref. 39:p. 92]. This truth is centered around the fact that conduction voltage of a MOSFET is higher and increases with voltage rating. It generally implies that a BJT is a more efficient device at low frequency in low voltage applications. Switching losses impair MOSFET operation only at frequencies above several hundred kHz. Switching losses in a BJT become more prevalent and surpass MOSFET conduction loss only at progressively higher frequencies. When comparing total power loss per unit area or maximum current density in each device as a function of frequency by adding switching losses to conduction losses, the crossover point, as illustrated in Figure 4.9 occurs at approximately 10~60 kHz, depending upon given conditions [Ref. 33:p. 217, Ref. 36:p. 1, Ref. 37:p. 14].

G. SAFE OPERATING AREA AND DRAIN-TO-SOURCE BREAK-DOWN VOLTAGE

Another item worth noting in Table 4.1 is the SOA (Safe Operating Area) of a BJT in comparison to a power MOSFET. An SOA graph is shown in Figure 4.10 defining the maximum values of current and voltage for each device at a given continuous rating. A power MOSFET will undergo avalanche breakdown if its applied drain-to-source voltage exceeds its maximum voltage rating, BV_{DSS} ; however, its

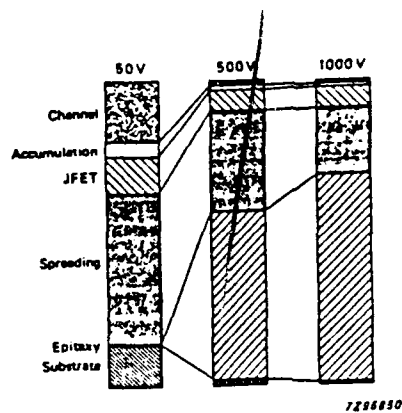


Figure 4.8: Power MOSFET Components of $R_{DS(on)}$ [From Ref. 38]

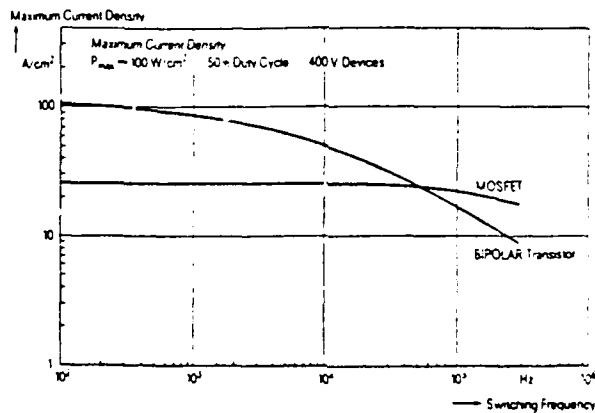


Figure 4.9: Maximum Current Density as a Function of Switching Frequency for MOSFETs and Bipolar Transistors Rated at 400 V [From Ref. 36]

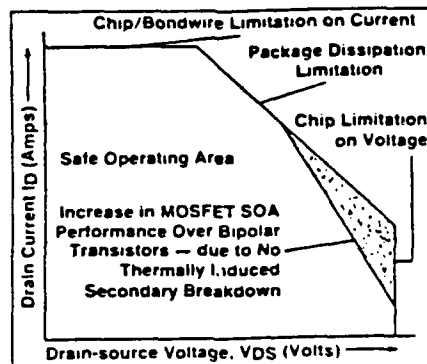


Figure 4.10: The Safe Operating Area of Assembled Power MOS and Bipolar Transistors [From Ref. 33]

secondary breakdown is small and incommensurable to that of a BJT. SOA's of a MOSFET are energy dependent and determined by thermal considerations only. A MOSFET, being a majority carrier device, has a positive temperature coefficient of forward resistance, which prevents localized hot-spots by forcing a uniform current distribution to occur across the total area of the device. It is a mechanism which inhibits thermal runaway. Virtual absence of secondary breakdown during forward or reverse bias makes the MOSFET a much more rugged device, giving it a much higher peak current carrying capability [Ref. 9:p. 2.44, Ref. 35:p. 95]. [Ref. 43:p. 125]

Second breakdown in a BJT refers to the fact that collector voltage is swiftly collapsing at the onset of failure [Ref. 46:p. 430]. It is characterized by the voltage dropping hundreds of volts in a few nanoseconds, accompanied by an increase in collector current. BJTs are prone to thermal runaway. Once started, this process becomes regenerative, higher current leads to higher temperatures, which in turn

causes higher current, etc. High peak currents are self destructive. They will pull a BJT out of saturation and cause it to overheat. A BJT undergoing secondary breakdown will not operate at full current and voltage, regardless of the power handling capability of its package. To avoid this condition, its possible SOA of voltage and current combinations are limited, especially at higher frequencies. The SOA of a BJT is therefore very much inferior to that of a MOSFET. [Ref. 9:p. 5.83, Ref. 12:pp. 15, 17, Ref. 33:p. 14, Ref. 45:pp. 131-132]

To make the sustaining voltage of a BJT equal to the breakdown voltage of a power MOSFET, BJT collector region thickness and resistance can be increased. But, this change in the device will cause the amount of voltage drop in the on-state to increase and degrade its performance. [Ref. 33:p. 218]

V. SYNTHESIS OF AN OPTIMUM SWITCH-MODE REGULATOR

A. CURRENT WAVEFORM DESIGN

Use of this theory, as discussed thus far, would be considered practical if, when given a set of simple design specifications, one could quickly describe the resulting circuit configuration and current waveform. After completing a few standard calculations, a judgement could then be made on the trade-offs a particular design would offer over another, in an attempt to minimize conduction loss.

As an example, the process is outlined for the development of the ramp-sine current waveform. The basic requirements and restrictions delineated in Table 5.1 are used to illustrate the characteristics of an input bus to which a dc-dc converter could be attached in a satellite.

Twenty-eight volts is a typical input voltage common to most DoD-sponsored unregulated-bus-voltage satellite power systems. A rated voltage of approximately 14 volts and 14 watts of power at the load output end is selected to emphasize the importance of this approach under low voltage and relatively high current conditions. Efficiency is dependent upon output voltage. High efficiency is difficult to obtain when either input or output voltages are low, comparable to switching element and voltage drops. Higher output voltages (i.e., 28 volts vs. five volts) result in much higher overall efficiencies. Electrical currents are not as large, conductor size and weight decrease accordingly, and distribution losses decrease in proportion with set power level and distance. In addition, semiconductor losses are proportionally less and the resultant heat produced is less difficult to dissipate. [Ref. 47:p. 181]

To maintain design simplicity and easily view its switch-current waveform, only one switching element is allowed. Paralleling semiconductor devices can pose a dynamic current sharing problem, due to a mismatch in switching speeds [Ref. 21:p.63]. Typical state-of-the-art resonant-mode dc-dc converters in production today, which quite commonly operate within the 100~ 300 kHz region, utilize single power MOSFETs. The value of 100 kHz is chosen as a maximum operating frequency to prevent dominance from transient switching losses. A minimum switching frequency of 20 kHz is established to prevent the switching element from functioning in the range of human detectable audio tones.

Besides knowing the circuit input and output voltage and power requirement, which establishes a majority of the buck operating characteristics, a switch on-time for the device must be selected. The on-time, in proportion to the switching frequency, governs the peak current value for each section of the combination Buck/ZCS, Quasi-Resonant Buck converter.

In a Quasi-Resonant dc-dc power converter, the on-time of the device is determined strictly by the natural frequency of the resonant tank. To achieve an optimum efficiency, a constant on-time must be sustained. Proper voltage regulation is maintained by altering the duty cycle to vary the switching frequency.

A fixed amount of switch on-time is important from a standpoint that it simplifies overall circuit design. Knowing this value, in fact, helps determine the amount of energy that can be consistently stored within the resonant and buck inductors. The design engineer is then better able to realize the size of each component he or she must supply to accommodate the most extreme load and line conditions existing over a wide range of switching frequencies.

To discover the maximum value attained by each of the individual ideal current waveforms in this type of design, the following assumptions must first be made:

TABLE 5.1: DC-DC Converter Baseline Requirements

<u>OUTPUT SPECIFICATIONS</u>	
Output voltage	14 VDC
Output power	14 W
<u>INPUT SPECIFICATIONS</u>	
Input voltage	28 V (unregulated)
Input voltage range	22~30 V
<u>GENERAL SPECIFICATIONS</u>	
Switching frequency	20~100 kHz
Single switching element	MOSFET
Single output	
Simple and minimal control circuitry	
Frequency control of output voltage	

- All phases of the resonant current waveform are considered to be sinusoidal; linear or quasi-sinusoidal periods of time T_{10} and T_{32} are ignored.
- The maximum peak buck current is one and one-half times greater than the peak resonant current.
- The half period of the quasi-resonant current waveform is equivalent to roughly 52% of switch on-time ($x = 0.52$).
- Only the lossless case is considered; the conditions previously stated in Chapter III, Section 3B, are upheld.

To calculate both the peak buck and peak resonant current values, an approximation citing the average current contribution by each waveform is needed. The average resonant input current, as viewed by the switch, is represented by

$$I_{swavg} = \left[\frac{2}{\pi} I_{rpeak} \left(x \frac{\tau}{T} \right) + \frac{1}{2} I_{Bpeak} \left(\frac{\tau}{T} \right) \right] \quad (5.1)$$

Solving this equation for a given average input current of P_{in}/V_{in} [amperes] over a period of T [sec] requires a peak buck current of,

$$I_{Bpeak} = 1.388 I_{swavg} \left(\frac{T}{\tau} \right) \quad (5.2)$$

$$= 1.388 \left(\frac{P_{in}}{V} \right) D \quad (5.3)$$

and a peak resonant current of,

$$I_{rpeak} = 0.922 I_{swavg} \left(\frac{T}{\tau} \right) \quad (5.4)$$

$$= 0.922 \left(\frac{P_{in}}{V} \right) D \quad (5.5)$$

The peak resonant current is a critical value which drives the selection of all other resonant tank parameters. From Equations 3.38 and 3.48, an expression can

be formed for either reactive energy storage element in terms of input voltage, peak resonant current, and half resonant period, that being

$$L_r = \frac{V}{I_{r_{peak}}} \left(\frac{0.52\tau}{\pi} \right) \quad (5.6)$$

and

$$C_r = \frac{I_{r_{peak}}}{V} \left(\frac{0.52\tau}{\pi} \right) \quad (5.7)$$

This, in turn, sets the resonant circuit characteristic frequency and determines the average resonant current out, I_L , as illustrated by Equations 3.40 and 3.57, respectively. Time intervals T_{10} , T_{21} , T_{32} , T_{43} , and T_{54} , are then easily defined by employing Equations 3.37, 3.39, 3.48, 3.52, and 3.53.

In trying to determine the correct inductor size value in the Buck circuit, a quick decision can be made if Equation 3.13 is used. This relationship established during the inductor charge interval is written as

$$L_B = 00.720 \left(\frac{\tau^2}{T} \right) \frac{(V - V_{out})}{I_{s_{avg}}} \quad (5.8)$$

Similarly, the Buck circuit discharge interval, D_2T , using Equation 3.14 can be expressed as

$$D_2T = \tau \left[\left(\frac{1}{M} \right) - 1 \right] \quad (5.9)$$

The remaining computations involving the discontinuous time interval and other critical parameters, which are an important concern in boundary condition determination, are prosaic with knowledge of load condition and period, T .

The power contributed to the load by each section is driven by the apportionment of input current after it passes through the power switching element. Roughly speaking, a 2:1 ratio is observed with the Buck circuit supplying approximately 70% of the circuit's raw power. Current through each individual element is elevated in inverse proportion to M .

B. CONVERTER ARCHITECTURE

As shown in Figure 5.1, a combination Buck/ZCS, Quasi-Resonant Buck dc-dc converter designed to function in its half-wave mode of operation was breadboarded. The voltage and current waveforms produced by this dc-dc power converter were observed at roughly 20% of full load condition or 11.2 ohms of resistance. System input voltage was held constant at 28 volts dc. By design, all boundary conditions identified for an open loop configuration in Table 3.1 were rigorously met, without exception.

1. Switching Element

A BUZ-60 N-channel enhancement mode power transistor was selected as the switching element having a drain-to-source resistance value of one ohm. A 10 volt peak-to-peak driving pulse, having a pulsewidth of 7.5μ -seconds with a periodicity of 22μ -seconds, was chosen as the input to the gate drive circuit. A small resistor, R_G , was inserted between pin 5 of the pulse transformer and the gate of the power MOSFET. This action was necessary to dampen the parasitic ringing oscillations which occurred intermittently during switch turn-on and turn-off intervals in time.

2. Gate Drive Circuit

A class B output stage, shown in Figure 5.2, was selected as the power MOSFET driving element based primarily upon the switching speed of each individual transistor, simplicity, the number of components required to implement the device, and a strong need to isolate the switching element from severe parasitic ringing incurred by use of the gate drive itself. The motivation behind this design was quite simple, to offer a very practical I.C. controller capable of presenting a very fast current sourcing and sinking action to the gate capacitances. Because a large current pulse can be drawn out of the gate in either state in a short amount

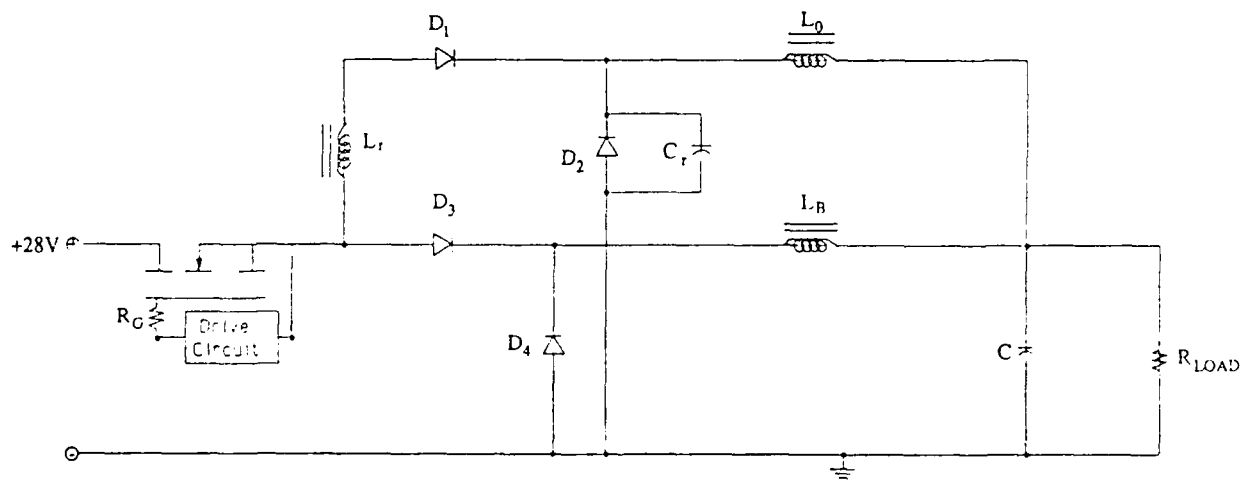


Figure 5.1: Buck/ZCS, Quasi-Resonant Buck DC-DC Converter

of time, saturation losses become tolerable and conduction losses in the on-state are better controlled. The gate drive is isolated from the switching element by incorporating a pulse transformer. This transformer, having a one-to-one turns ratio, was connected in phase providing the necessary isolation from line to the load. The output impedance of the circuit was minimal, lowered through the use of a single NPN and PNP complementary symmetry emitter-follower, resulting in a higher switching speed.

3. Nonlinear Elements

To implement the half-wave mode ZCS, Quasi-Resonant converter, a L -type current-mode switch was utilized. A fast recovery diode, D_1 , having a maximum reverse recovery time ten times greater than that of the MOSFET device, was used to prevent the backflow of energy into the source and to minimize diode peak recovery current.

In the Buck converter section, both freewheeling diodes, D_3 and D_4 , were selected as Schottky barrier diodes, having an instantaneous voltage drop of less than three-tenths of a volt for seven-tenths of an ampere of instantaneous forward current. Realistically speaking, in either case, the corresponding average forward power dissipation represented a maximum power loss of well less than one-quarter watt per diode.

C. MODEL ANALYSIS

This analysis is offered as a succinct summary to the Buck/ZCS, Quasi-Resonant switching converter due to previous discussion borne in Chapter III. The resulting behavior of the switch-current waveform is in agreement with the supposition, with few exceptions. A complete switching cycle, T , in this combination converter is apportioned into six different operating modes. As demonstrated in:

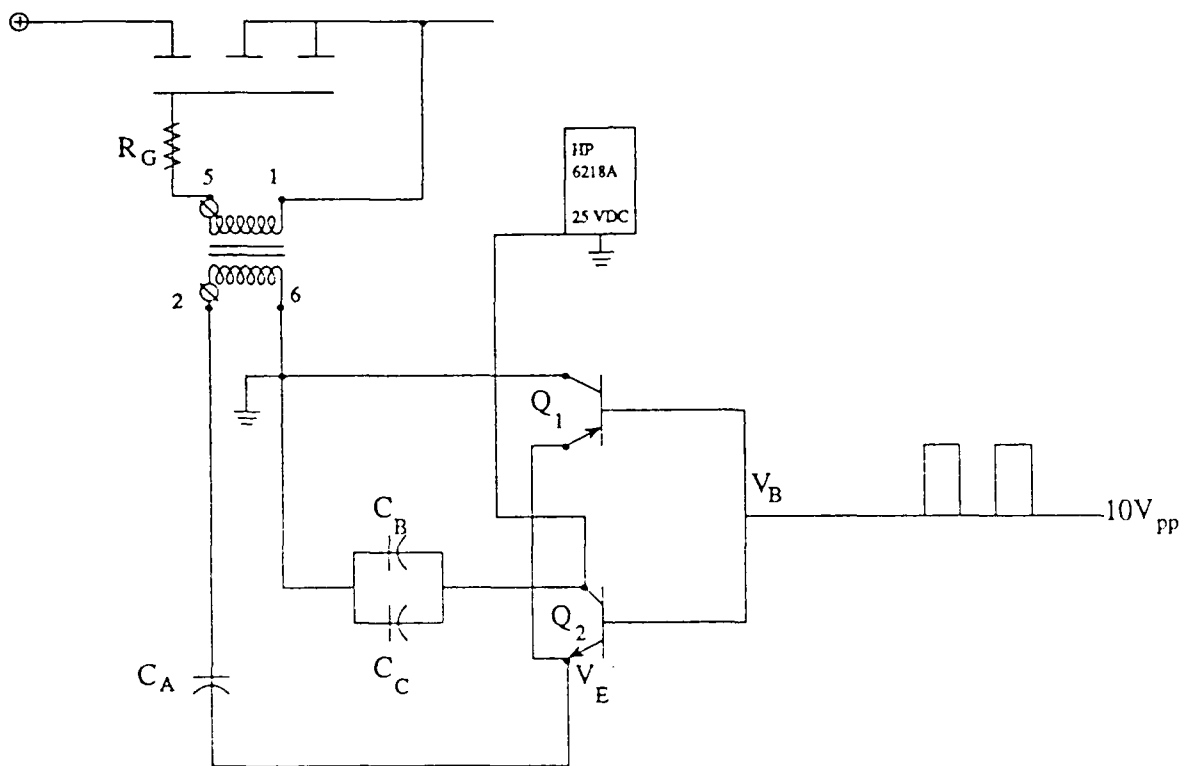


Figure 5.2: Class B Output Stage Type Gate Drive

Figure 5.3, the individual waveforms contained in illustrations within this chapter are similar in shape to standard resonant and PWM discontinuous mode converter waveforms; however, their combined form, timing, and current values share a special predetermined relationship.

1. MODE I - Inductor-Charging State

When the power MOSFET is turned on, both diodes, D_1 and D_3 , become forward-biased as a positive current is applied. Energy in both Buck and quasi-resonant inductors is allowed to build as the ideal diodes behave as a short circuit in the forward direction with zero voltage drop. Once again, inductor current is not permitted to resonantly charge the resonant capacitor, C_r , until the resonant current, $I_{Lr}(t)$, surpasses the constant current $I_{Lo}(t)$, supplied by the very large inductor, L_o . As a result of this phenomena, the instantaneous switch current, $I_{sw}(t)$, will equal the instantaneous load current, $I_L(t)$, i.e.,

$$I_{sw}(t) = I_L(t) = I_{LB}(t) + I_{Lo} \quad (5.10)$$

where

$$I_{LB}(t) = \frac{(V - V_{out})}{L} t \quad (5.11)$$

as long as the switch remains closed.

2. MODE II - Resonant/Buck Inductor-Charging State

This mode marks the beginning of the resonant charging cycle in the quasi-resonant converter half-circuit as diode, D_2 , is commutated off. As demonstrated in Figure 5.4, no change occurs in the anticipated physical appearance of the Buck converter individual waveform. The total instantaneous switch current becomes non-linear at this point. The total instantaneous switch current put through

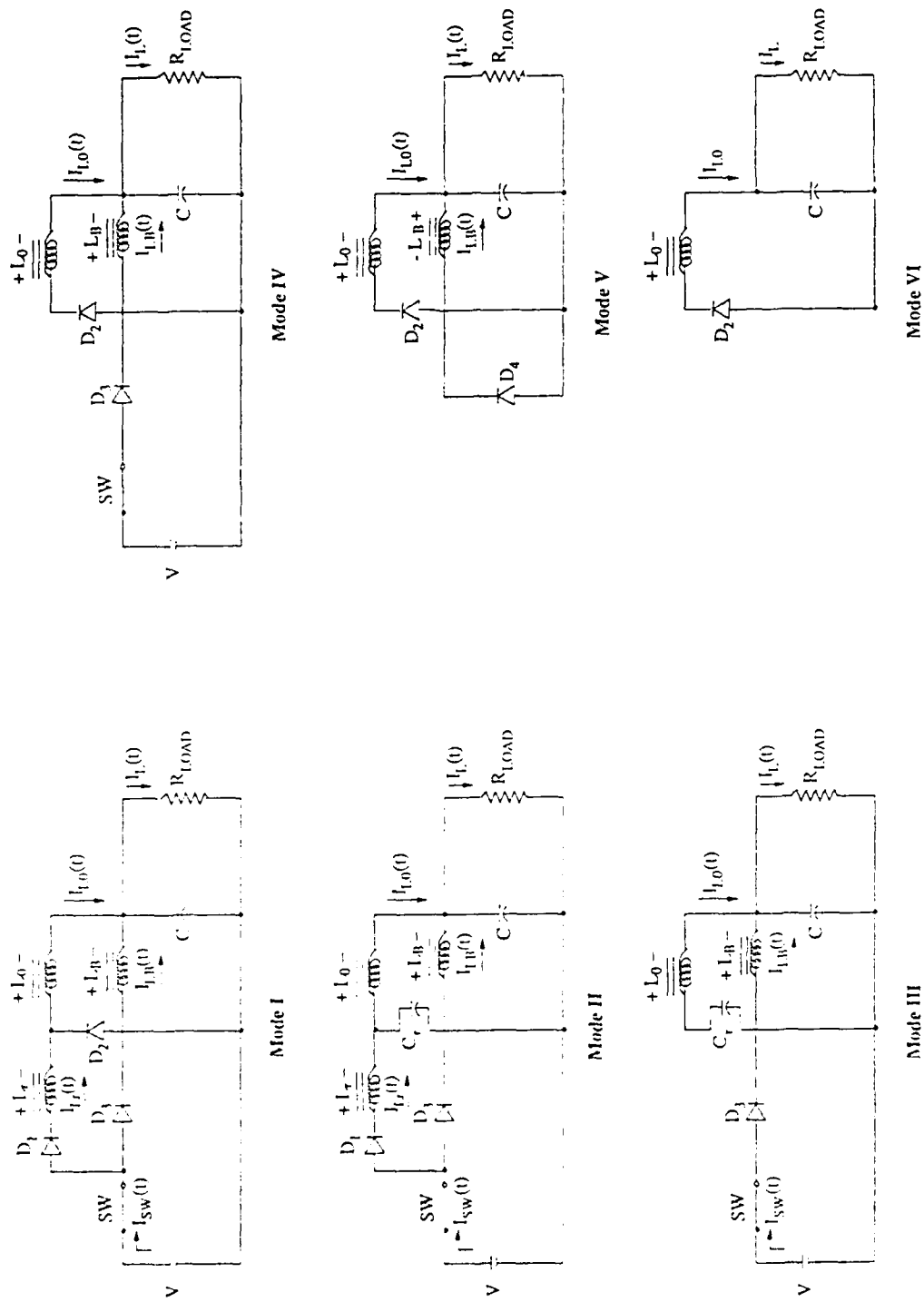


Figure 5.3: Six Modes of a Buck/ZCS, Quasi-Resonant Buck DC-DC Converter

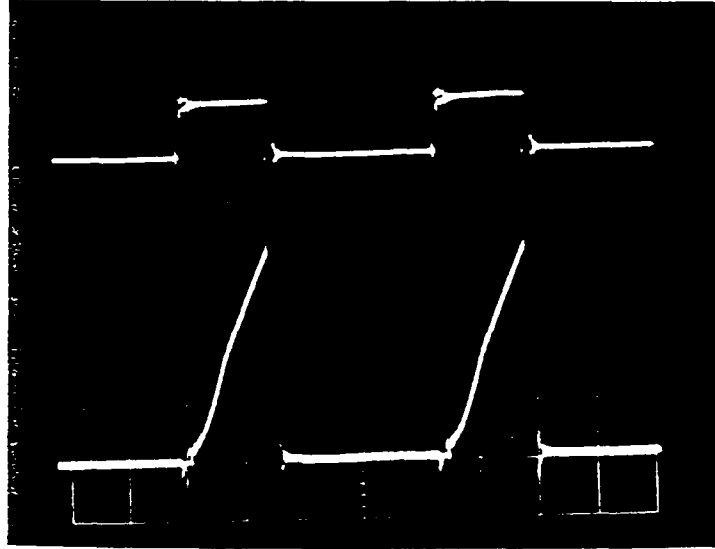


Figure 5.4: Buck Inductor Charging Current Waveform, $T = 22 \times 10^{-6}$ [sec], $R_{LOAD} = 11.2$ [Ω], Top waveform: Gate Drive Pulse (10 Volts/div), Bottom waveform: $I_{LB}(t)$ (1 amp/div)

the switch is

$$I_{sw}(t) = I_{LB}(t) + \frac{V}{\sqrt{\left(\frac{L_r}{C_r}\right)}} [\sin wt] + I_{L_o} . \quad (5.12)$$

As the opportunity presents itself, the resonant inductor first, and then the resonant capacitor, both charge to their maximum value during this time interval. As depicted in Figure 5.4, the peak resonant current reached is 1.4 amperes. Likewise, the resonant capacitor attains a peak value of 51 volts, which is nearly equivalent to $2V$ in measure. When $I_{L_r}(t)$ equals $I_{L_o}(t)$ again, C_r discharges its reservoir of energy into the load.

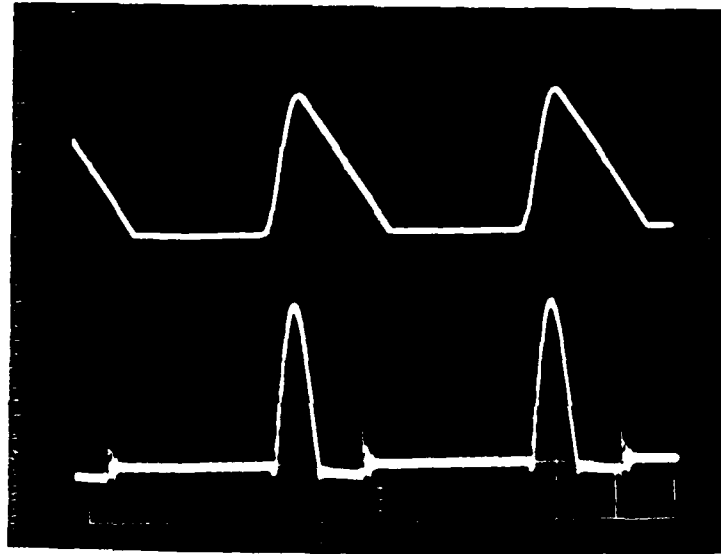


Figure 5.5: Resonant Waveforms, $T = 22 \times 10^{-6}$ [sec], $R_{LOAD} = 11.2$ [Ω], Top Waveform: V_{Cr} (20 Volts/div); Bottom Waveform: I_{Lr} (1 amp/div)

3. MODE III - Resonant Capacitor-Discharging/Buck Inductor-Charging State

This mode reveals, that as soon as diode D_1 terminates resonant inductor current flow, both the resonant capacitive voltage waveform, as well as the switch current waveform, become linear in nature. The switch current is equal to buck current. This action, as it prevents negative current oscillations, permits an easy calculation to be completed using the graph in Figure 5.5(b) to determine the average resonant current out, I_{Lo} , using Equation 3.49. The average resonant current out, over period T , results in being equivalent to 0.300 amperes.

4. MODE IV - Resonant-Freewheeling/Buck Inductor-Charging State

After all resonant capacitive energy is expended, the total instantaneous switch current remains a simple function of the buck inductor charging current alone. The portion of the instantaneous switch current developed throughout the inductor-charging state of the Buck circuit is stipulated by Equation 3.13 for Modes I, II, and III alike. The resonant-freewheeling/Buck Inductor-Charging State lasts until turn-off of the power MOSFET at time T_5 .

5. MODE V - Resonant Freewheeling/Buck Discharge-State

At time τ , as predetermined, the power MOSFET is switched off by the gate drive. Diode D_4 is commutated on as the buck inductor, L_B , reverses its field polarity. The instantaneous current waveform, as viewed by the semiconductor switch up to time T_5 , is shown in Figure 5.6. The absolute maximum peak current observed, which must be handled by the majority carrier switching device at turn-off is 2.05 amps. The computed average current contribution, using Equation 3.11, given by the buck inductor current waveform in Figure 5.7 to the load is 0.769 amperes.

Mode V is distinguished from other modes of operation by the placement of an additional diode, D_3 , prior to the buck inductor to guarantee proper converter operation. Without its presence, any discharge of energy from L_o or L_B into the resonant tank would prematurely permit the charging of the resonant circuit and disrupt the requisite converter state waveshaping function.

6. MODE VI - Resonant-Freewheeling/Buck Discontinuous State

Mode VI, the final mode, is identical to the ZCS, Quasi-Resonant Buck converter freewheeling stage discussed in Chapter III, Section B, Subsection 3. This

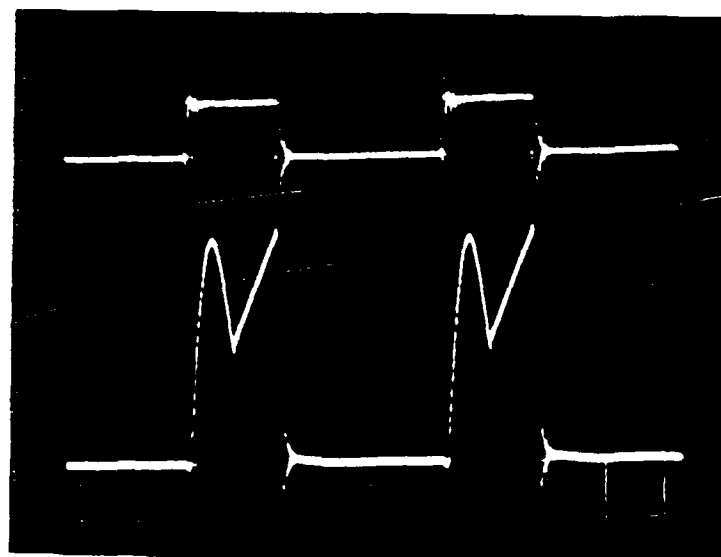


Figure 5.6: Drain-to-Source-Current Waveform, $T = 22 \times 10^{-6}$ [sec], $R_{LOAD} = 11.2$ [Ω], Top Waveform: Gate Drive Pulse (10 Volts/div), Bottom Waveform: I_{DS} (1 amp/div)

mode is characterized by the magnitude of inductor, L_o , and length of interval D_3T . The magnitude of D_3T is a direct function of:

$$D_3T \sim f\left(R, T, \frac{1}{D}, \frac{1}{L}\right) \quad (5.13)$$

D. CONDUCTION LOSS MODEL - SUMMARY

Overall, after viewing Figures 5.4 and 5.5, the ratio of peak buck to peak resonant current matches up quite well with proposed theoretical values, showing a difference of less than 3%. Despite a loss in output power of 1.85 watts, this non-ideal converter as illustrated in Figure 5.8 is still able to provide to the load 1.07 amperes of output current. Having achieved this necessary agreement in peak current value for both quasi-resonant and buck current waveforms permits use of Equation A1.1 to estimate conduction loss.

The rms current squared during MOSFET switch on-time is closely approximated using Equation A1.2, time intervals T_{10} and T_{32} occupy less than 10% of the quasi-resonant current waveform half period. A value of 0.803 milli-watts is dissipated in power as a result of the BUZ-60 device having to transfer one-half ampere of input current through one ohm of resistance.

At this point, a good comparison can be made between conduction loss and all other dissipative losses occurring during this same time period. The motive here is to understand the huge burden conduction loss places on circuit efficiency under this loading condition. To assimilate the difference in magnitude of switching loss requires the assistance of Equation 4.5.

$$P_{swon} = \frac{1}{2} f_s C_{oss} V_{DS}^2 \quad (5.14)$$

Using a maximum output capacitance of 180 pf, as noted on the product summary sheet, and adding an additional 5 pf to compensate for stray capacitance yields a loss of 3.39 milli-watts.

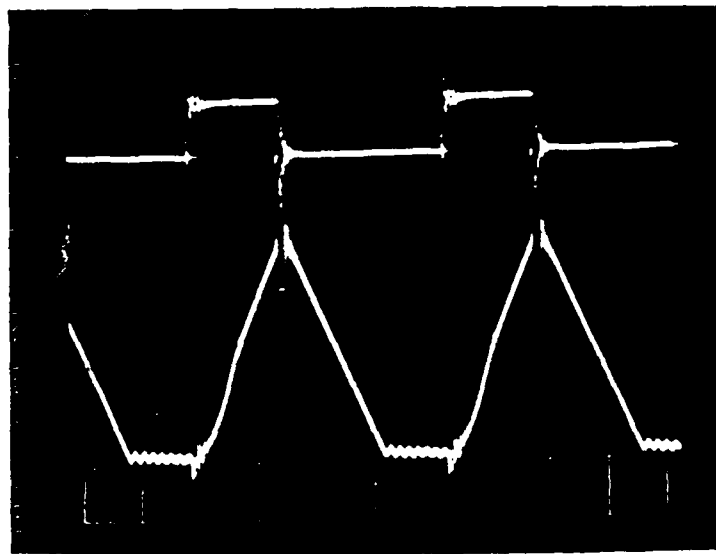


Figure 5.7: Buck Inductor Charging/Discharging Current Waveform, $T = 22 \times 10^{-6}[\text{sec}]$, $R_{LOAD} = 11.2 [\Omega]$, Top waveform: Gate Drive Pulse (10 Volts/div), Bottom waveform: $I_{LB}(t)$ (1 amp/div)

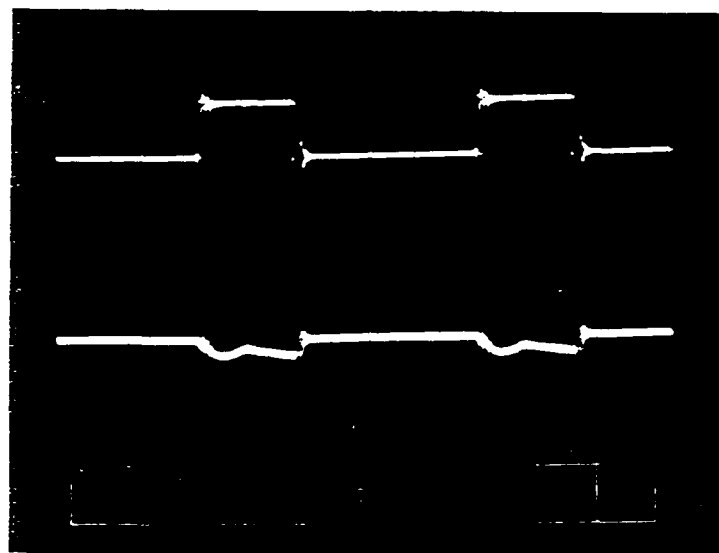


Figure 5.8: Current Waveform Through the Load Resistor, $T = 22 \times 10^{-6}$ [sec], $R_{LOAD} = 11.2$ [Ω], Top waveform: Gate Drive Pulse (10 Volts/div), Bottom waveform: $I_L(t)$ (1 amp/div)

The other loss which can be accounted for is the power loss due to drain-to-source leakage. This loss is also small, causing 74 milli-watts of power loss from four milli-amperes of leakage current.

Therefore, as expressed before, under a high current, low voltage condition, such as in a satellite:

$$P_{cond} \gg P_{sw} + P_L \quad (5.15)$$

Using this finding, it can be stated that if a ramp-sine waveform is subject to a conduction loss of 0.808 watts, then a ramp waveform in its self will support an even greater amount of dissipation of 0.958 watts. Furthermore, a ramp-sine-sine current waveform under the tradeoff of additional circuitry would cause this loss to decline even further in value to approximately 0.720 watts of power.

VI. CONCLUSION

The high cost of placing a satellite into orbit has imposed severe constraints upon the entire power system design philosophy. The desirable effects produced from reduced cost, less power loss, and size and weight limitations are now a constant theme in any effort to produce effective power conversion equipment. An efficient power switching technique, as proven in this research, is definitely the most successful method in meeting the substantial demand for increased power system density today.

To alleviate power dissipation losses in a dc-dc converter, the concept of current waveform waveshaping was introduced and implemented for power processing circuits. Using a quasi-Newton numerical technique, an analysis was performed to identify the physical relationship existing between the peak currents of various combined current waveforms. Theoretically, the ramp-sine-sine relationship produced the current waveform with the lowest overall conduction power loss.

To enhance the understanding of fundamental principles underlying the circuit operation of different elementary current waveforms, a complete dc analysis was presented on two non-dissipative power systems. Imperative to this study was the ability to develop and comprehend the proper current and voltage relationships which correctly define the condition of resonance and discontinuous conduction mode of converter operation. Also, in a summary, a comparison between the MOSFET and the BJT switching elements was made. The basic static and transient switching properties of each transistor were investigated to identify the strong and weak points of each semi-conductor switch. In most cases, it was obvious that the capabilities offered by a majority-carrier device were far superior to advantages of a

BJT. The detrimental power losses facing each device, especially MOSFET-plaguing conduction loss, were carefully scrutinized.

The simplest and perhaps the most widely used variety of switch-mode regulator was then breadboarded to prove the feasibility of this study. A step-down 45 kHz, 14 volt, 14 watt, Buck/ZCS, Quasi-Resonant Buck dc-dc converter using a BUZ-60 power MOSFET provided results which were consistent with the theory proposed. It established a basis that this design concept is applicable to a variety of conventional converters in two ways. First, it proved that the goal of producing any of the displayed waveforms illustrated in Figures A.3 through A.6 is possible using existing technology. Secondly, it demonstrated that the resonant switch concept can be applied to a host of other basic switcher designs operating in their discontinuous conduction mode as well.

Development of a MOSFET power converter for use at low voltage and high current levels has been limited because other semiconductor devices functioning in the frequency domain from 20 ~ 100 kHz operate more efficiently. Thus, unfortunately, techniques in this area have not yet been given the opportunity to achieve their full development. However, as proven in this research, prospects exist for the maturation of a more highly efficient dc-dc converter by using certain circuit devices and physical waveshaping techniques. The highlights and merits of using the design process disclosed in this thesis are:

- An increase in power conversion frequency above the 20 kHz frequency plane with a growth in power system density and a depreciation in conduction loss.
- Improved design flexibility without adding significantly to the current stress which occurs in the power switch.

- Implementation of a half-wave mode, ZCS, series-resonant, *L*-type, switch topology to preserve energy that which would otherwise be dissipated in conduction loss through the anti-parallel diode under different load conditions in a full-wave mode type of quasi-resonant converter.
- Natural commutation of quasi-sinusoidal component current waveforms.
- Added energy conservation and space saving in a dc-dc converter because of its small size, light weight, and improved performance efficiency.

The comparative dc analysis of the operation of the Buck/ZCS, Quasi-Resonant Buck converter functioning in its discontinuous inductor current mode of operation is now complete. The performance of an experimental circuit built in the lab has verified the author's intuitive prediction concerning the relationship between conduction voltage drop and the shape of the current waveform passing through the switching element. It is thought that the simplicity behind this development and the insight it provides should make waveshaping a helpful tool to limit conduction power loss in future dc-dc converter analysis.

APPENDIX A: IMSL ROUTINE ZXMIN

A.1 PROGRAM SOFTWARE

The IMSL routine ZXMIN, contained within the enclosed FORTRAN program, which Section A-II, is used to predict the theoretical outcome of minimum average power to a combination of proposed waveforms. Items required to initiate this program are:

1. FUNCT, a user-supplied subroutine used to calculate the function F , which in this case, is the power minimization of $\left[\frac{(N+1)}{2}\right]$ waveforms.
2. X , a vector of length N , containing parameter values.
3. N , the number of variables or parameter estimates contained within F .
4. $NSIG$, the convergence criterion governing the degree of accuracy required in parameter estimates.

Given N initial parameter estimates supplied by the user of the FORTRAN program and the information above (including all other less significant arguments required by the calling sequence as well), the subroutine ZXMIN is called. ZXMIN uses subroutine FUNCT to first calculate F .

The function F is dependent upon the vector X for N different parameter estimates. The function F is found by first solving Equation 2.3 for each current waveform combination, and then determining the absolute value of one minus the average power dissipated, P , in the switch. Table A.1 gives the solutions to Equations 2.2 and 2.3 for each of the six waveforms analyzed. When P is computed for any current waveform, two assumptions are made. For each case concerned: (1) the

time, τ_2 , given for the longest duration single element waveform is always assumed to be equal to one; and (2) to lessen the number of independent values contained within F , one of the parameter values $x(1)$, $x(2)$, ..., $x(N)$ is always solved for Q equal to one in terms of the other remaining parameter values. These initial conditions simplify each expression and reduce the number of calculations involved. The convergence criterion required for the final iteration of F is specified to four significant digits.

Solutions for F were not necessarily determined to be unique. Also, due to the nature of the algorithm, as was in the case of the sine-sine-sine waveform, exact convergence of F was not achieved. Iterations were terminated due to rounding errors, or final parameter values resulted in negative values of $x(N)$. Therefore, the setting of initial conditions each time by the operator was influential in obtaining final results.

Figures A.1 through A.6 illustrate graphically the optimum power minimum for each current waveform combination examined. Given in each graph are the values of switch-on time, τ , versus current as a function of time, $i(t)$, for each individual current element waveform and their sum as well. It is important to note that, as the average power dissipated in the switching cycle decreases, the peak current of the combination is also reduced. The ramp-sine-sine waveform is proven to be the most efficient process. Table A.2 summarizes the results obtained for the overall analysis.

Table A.1: Basic Current Waveform Equations

A1.1	Ramp	$\frac{1}{2}\tau_1 I_1$	$\frac{1}{3}\tau_1 I_1^2$
A1.2	Sine	$\frac{2}{\pi}[\tau_1 I_1]$	$\frac{1}{2}\tau_1 I_1^2$
A1.3	Sine-Sine	$\frac{2}{\pi}[\tau_1 I_1 + \tau_2 I_2]$	$\frac{1}{2}[\tau_1 I_1^2 + \tau_2 I_2^2] + \frac{2I_1 I_2 \tau_1 \tau_2 \sin\left(\frac{\pi\tau_1}{\tau_2}\right)}{\pi(\tau_2^2 - \tau_1^2)}$
A1.4	Ramp-Sine	$\frac{2}{\pi}\left[\tau_1 I_1 + \frac{\pi}{4}(\tau_2 I_2)\right]$	$\frac{1}{2}\tau_1 I_1^2 + \frac{1}{3}\tau_2 I_2^2 + \frac{2\tau_1^2 I_1 I_2}{\pi\tau_2}$
A1.5	Sine-Sine-Sine	$\frac{2}{\pi}[\tau_1 I_1 + \tau_2 I_2 + \tau_3 I_3]$	$\frac{1}{2}[\tau_1 I_1^2 + \tau_2 I_2^2 + \tau_3 I_3^2] + \frac{4}{\pi}\left[\frac{\tau_1 I_1 \tau_2^2 I_3 \sin\left(\frac{\pi\tau_1}{\tau_3}\right)}{(\tau_3^2 - \tau_1^2)} + \dots\right]$ $\frac{\tau_1 I_1 \tau_2^2 I_2 \sin\left(\frac{\pi\tau_1}{\tau_2}\right)}{(\tau_2^2 - \tau_1^2)} + \frac{\tau_2^2 I_2 \tau_3 I_3 \sin\left(\frac{\pi\tau_2}{\tau_3}\right)}{(\tau_3^2 - \tau_2^2)}\left]\right.$
A1.6	Ramp-Sine-Sine	$\frac{2}{\pi}[\tau_1 I_1 + \tau_3 I_3] + \frac{1}{2}\tau_2 I_2$	$\frac{1}{2}[\tau_1 I_1^2 + \tau_3 I_3^2] + \frac{1}{3}\tau_2 I_2^2 + \frac{4I_1 \tau_1 I_3 \tau_3^2 \sin\left(\frac{\pi\tau_1}{\tau_3}\right)}{\pi(\tau_3^2 - \tau_1^2)} + \frac{2I_2}{\pi\tau_2}[I_1 \tau_2 + I_3 \tau_3^2]$

Table A.2: Waveform Results

WAVEFORM	I_p	P	Q	% REDUCTION RAMP
Ramp	2.000	1.333	1.0	0.00
Sine	1.571	1.234	1.0	7.43
Sine-Sine	1.395	1.147	1.0	13.95
Ramp-Sine	1.388	1.086	1.0	18.60
Sine-Sine-Sine	1.372	1.302	1.0	2.33
Ramp-Sine-Sine	1.171	1.001	1.0	24.90

RAMP POWER MINIMUM

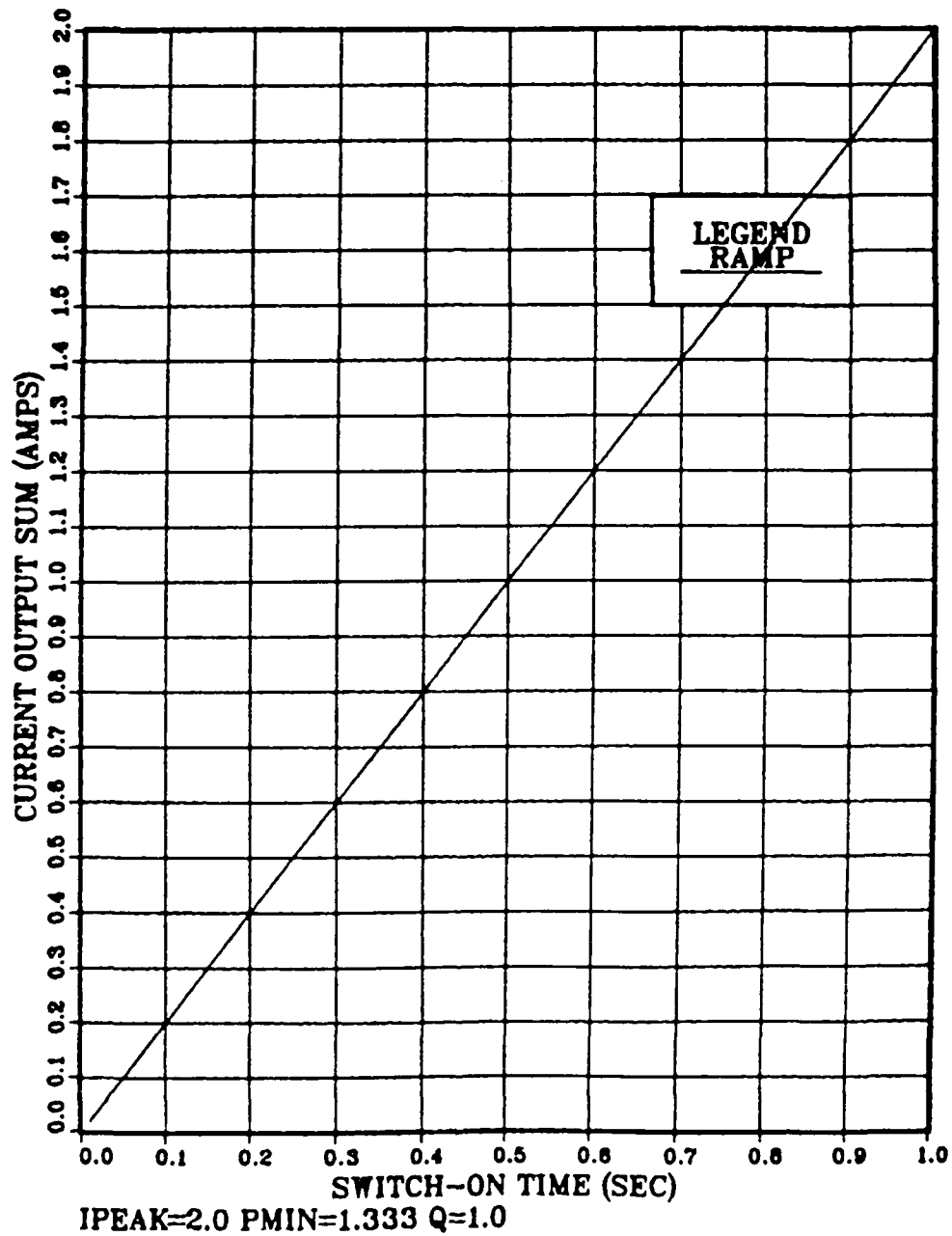


Figure A.1: Ramp Current Waveform

SINE POWER MINIMUM

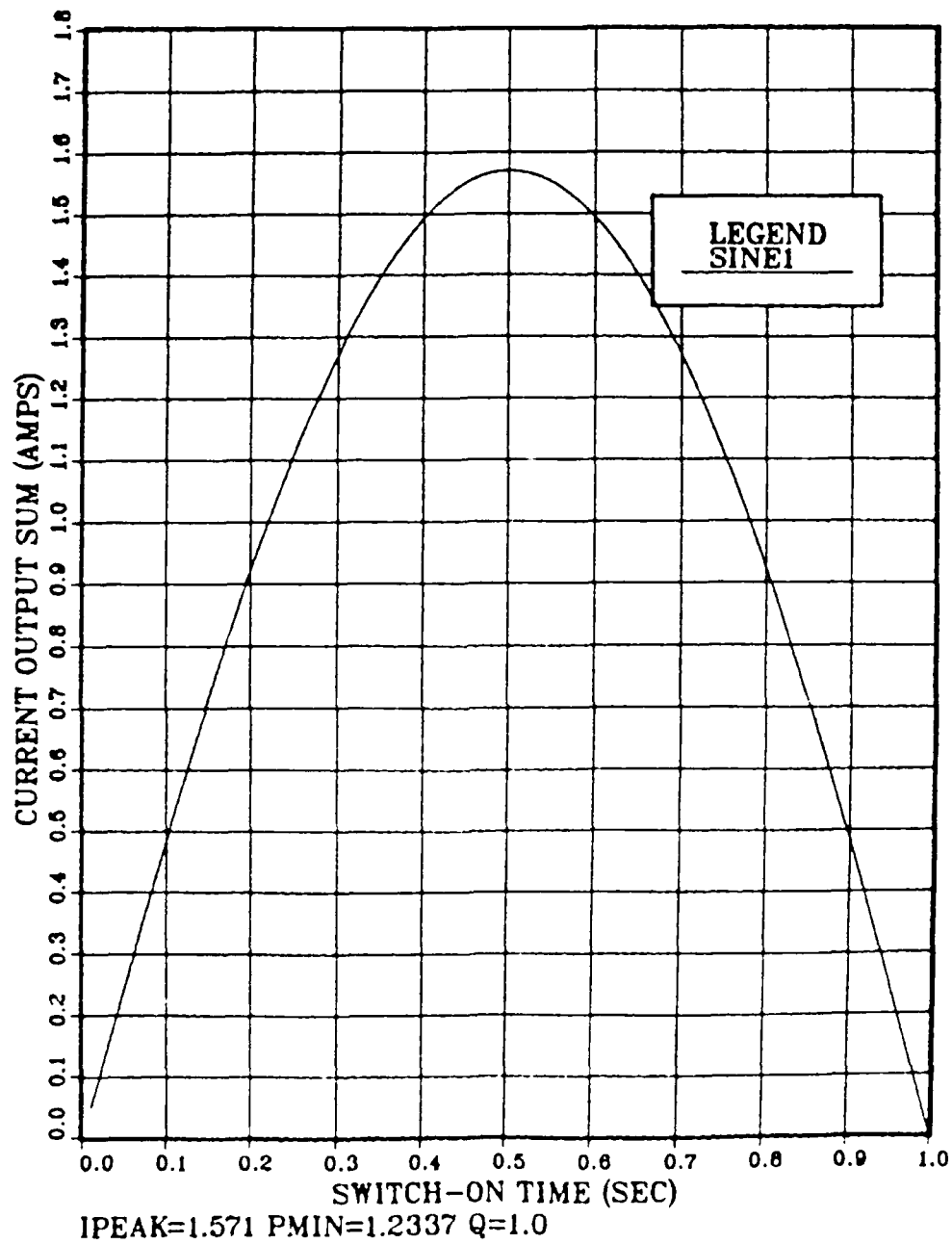


Figure A.2: Sine Current Waveform

SINE-SINE POWER MINIMUM

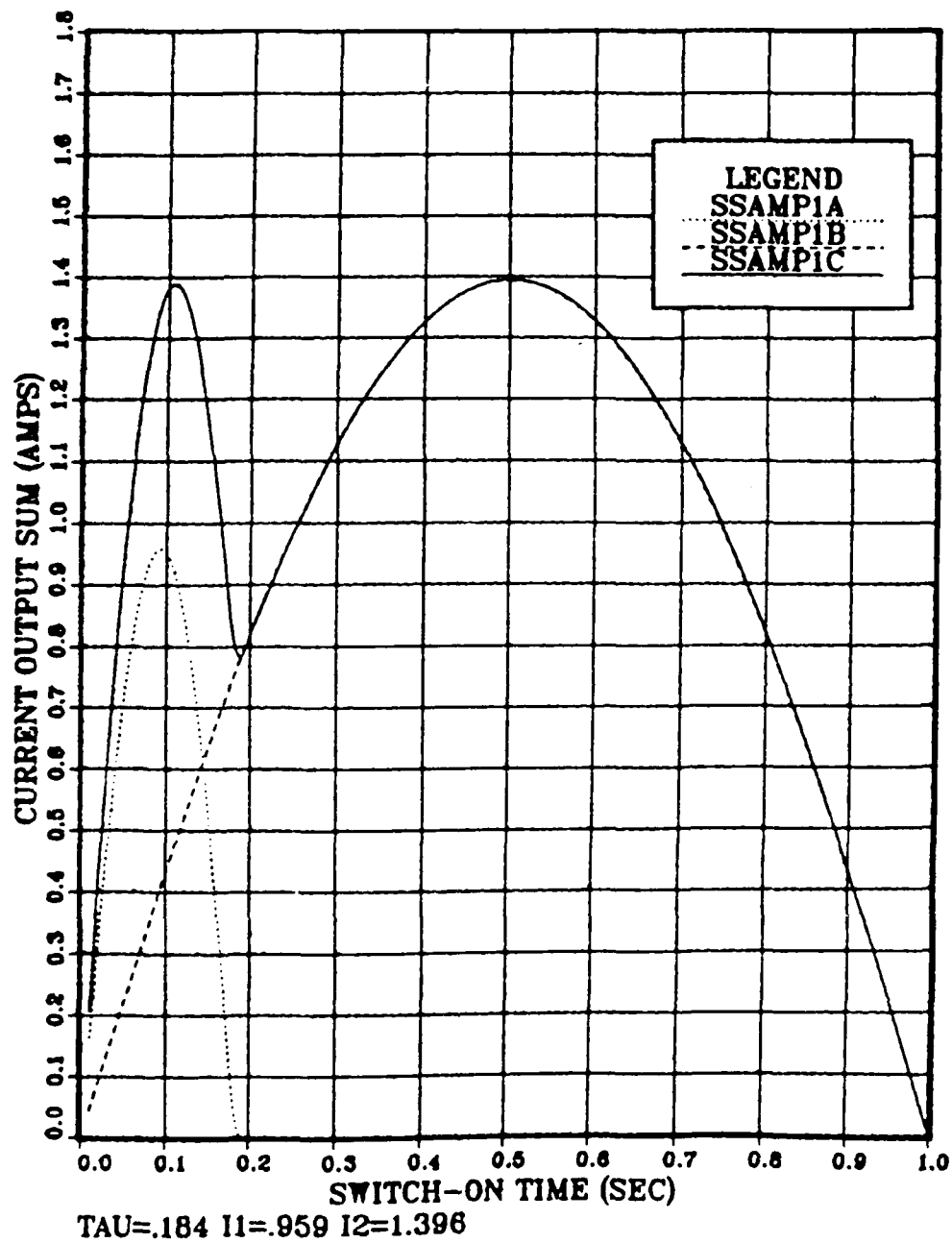


Figure A.3: Sine-Sine Current Waveform

RAMP-SINE POWER MINIMUM

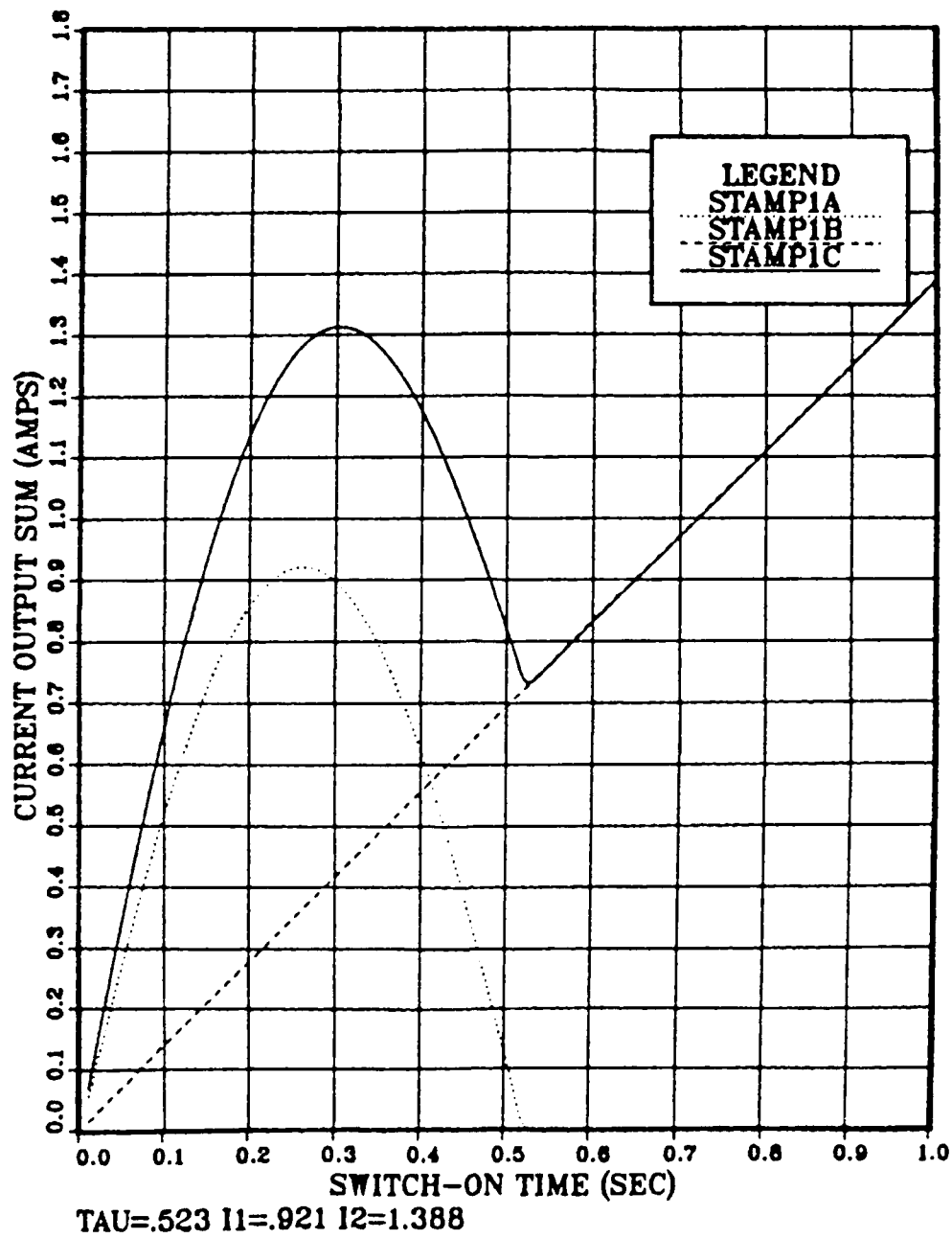


Figure A.4: Ramp-Sine Current Waveform

SINE-SINE-SINE POWER MINIMUM

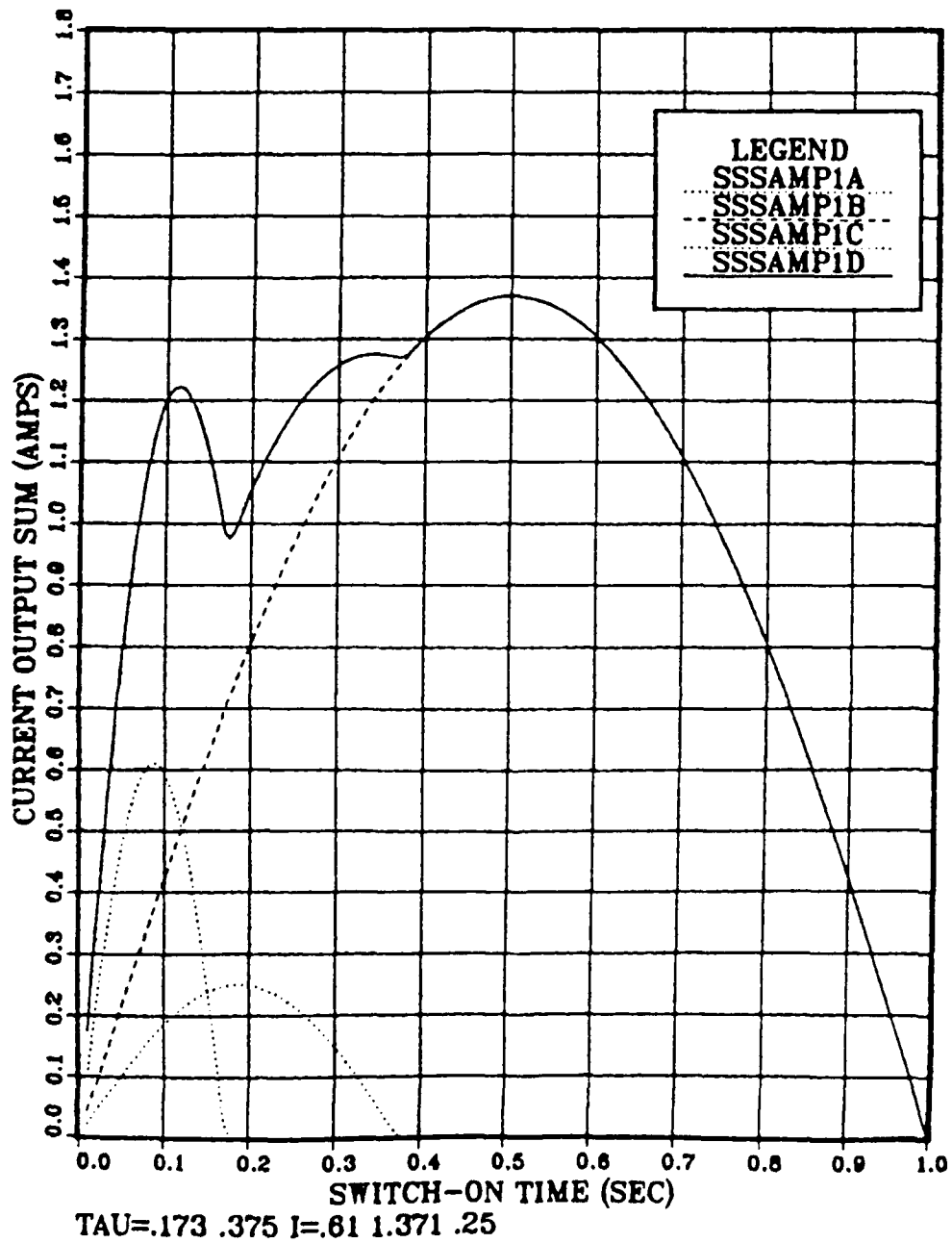


Figure A.5: Sine-Sine-Sine Current Waveform

RAMP-SINE-SINE POWER MINIMUM

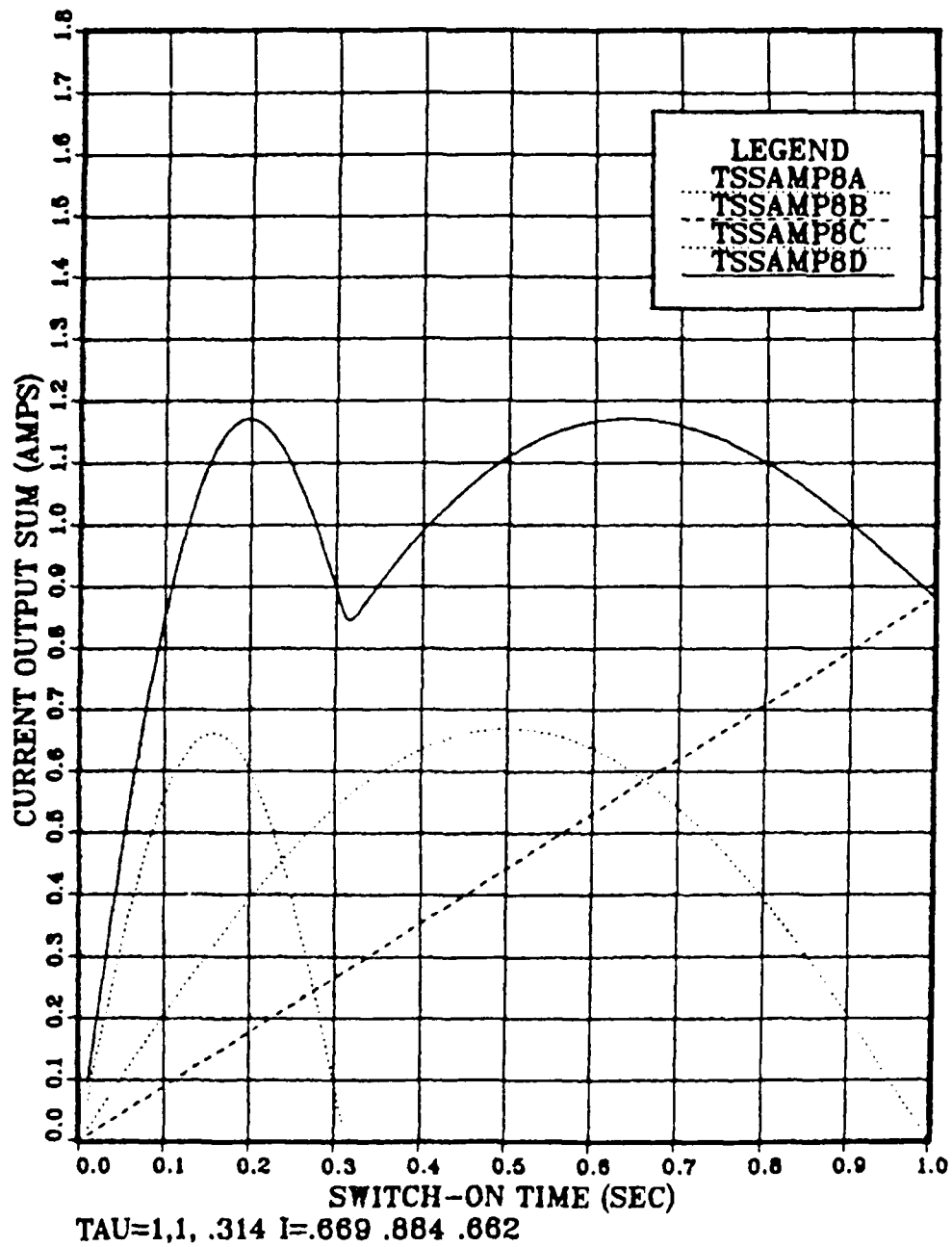


Figure A.6: Ramp-Sine-Sine Current Waveform

A.2 RAMP-SINE CURRENT WAVEFORM NUMERICAL RESULTS

This section contains the FORTRAN program to calculate the power minimization of different elementary waveforms. As configured, it is set up to determine the minimum power and peak current for the Ramp-Sine waveform. The subsequent table of numbers which follow are the result of the analysis performed and graphed in Figure A.4.

CS\$NOEXT		AMP00010
C		AMP00020
C		AMP00030
C		AMP00040
C	*****	AMP00050
C	* POWER MINIMIZATION OF CURRENT WAVEFORMS *	AMP00060
C	* DOUGLAS P. MILLER *	AMP00070
C	* 23 NOV 88 *	AMP00080
C	*****	AMP00090
		AMP00100
		AMP00110
C	THIS SIMPLE FORTRAN PROGRAM IS DESIGNED TO	AMP00120
C	DETERMINE THE THEORETICAL MINIMUM AVERAGE POWER	AMP00130
C	DISSIPATED BY A POWER MOSFET OVER ONE SWITCHING	AMP00140
C	CYCLE. THE AVERAGE AMOUNT OF CHARGE TRANSFERRED	AMP00150
C	DURING SWITCH ON-TIME, THE SWITCHING ELEMENT ON-	AMP00160
C	RESISTANCE, AND SWITCHING PERIOD ARE ALL NORMALIZED	AMP00170
C	TO EQUAL A VALUE OF ONE.	AMP00180
		AMP00190
C	*****VARIABLE LISTING*****	AMP00200
		AMP00210
C	F= SCALAR VALUE OF MINIMIZED FUNCTION AT FINAL	AMP00220
C	PARAMETER ESTIMATES.	AMP00230
C	FUNCT= A USER SUPPLIED SUBROUTINE WHICH CALCULATES	AMP00240
C	THE FUNCTION F FOR GIVEN PARAMETER VALUES	AMP00250
C	X(1), X(2), ..., X(N).	AMP00260
C	THE CALLING MATRIX HAS THE FORM	AMP00270
C	CALL FUNCT(N,X,F).	AMP00280
		AMP00290
C	G= VECTOR OF LENGTH N CONTAINING ON OUTPUT AN	AMP00300
C	ESTIMATE OF THE GRADIENT DF/DX(I), I=1,...N	AMP00310
C	AT FINAL PARAMETER ESTIMATES.	AMP00320
		AMP00330
C	H= VECTOR OF LENGTH N*(N+1)/2 CONTAINING AN	AMP00340
C	ESTIMATE OF THE HESSIAN MATRIX	AMP00350
C	D**2F/(DX(I)DX(J)), I,J=1,...N.	AMP00360
C	ON INPUT IF:	AMP00370
C	IOPT=0, 2, OR 3 ZXMIN INITIALIZES H.	AMP00380
C	IOPT=1 USER INITIALIZES THE SETTING OF H.	AMP00390
C	H IS NOT POSITIVE DEFINITE A TERMINAL ERROR	AMP00400
C	OCCURS.	AMP00410
C	ON OUTPUT CONTAINS ESTIMATE OF HESSIAN MATRIX	AMP00420
C	USING FINAL PARAMETER VALUES.	AMP00430
		AMP00440
C	IER= OUTPUT ERROR PARAMETER.	AMP00450
C	IER=0 CONVERGENCE ACHIEVED NO ERRORS.	AMP00460
C	IER=129 INITIAL HESSIAN MATRIX USED BY ZXMIN	AMP00470
C	IS NOT POSITIVE DEFINITE, EVEN AFTER	AMP00480
C	TRYING TO MAKE ALL DIAGONAL ELEMENTS	AMP00490
C	POSITIVE BY ADDING A MULTIPLE OF ITS	AMP00500
C	IDENTITY.	AMP00510
C	IER=130 ITERATION WAS TERMINATED DUE TO SIG-	AMP00520
C	-NIFICANT ROUNDING ERRORS. CONVERGENCE	AMP00530
C	CRITERIA OF PARAMETER ESTIMATES IS NOT	AMP00540
C	MET.	AMP00550

C	IER=131 PROGRAM TERMINATED BECAUSE MAXFN	AMP00370
C	EXCEEDED.	AMP00380
C	IOPT= OPTIONS SELECTOR, ON INPUT:	AMP00390
C	IOPT=0 CAUSES ZXMIN TO INITIALIZE THE HESSIAN	AMP00400
C	MATRIX H TO THE IDENTITY MATRIX.	AMP00410
C	IOPT=1 INDICATES USER HAS INITIALIZED H AS A	AMP00420
C	POSITIVE DEFINITE MATRIX.	AMP00430
C	MAXFN= MAXIMUM NUMBER OF CALLS TO SUBROUTINE	AMP00440
C	FUNCT ALLOWED.	AMP00450
C	N= THE NUMBER OF PARAMETER VALUES.	AMP00460
C	NSIG= THE NUMBER OF DIGITS OF ACCURACY REQUIRED IN	AMP00470
C	THE PARAMETER ESTIMATES. THIS VALUE GOVERNS	AMP00480
C	THE CONVERGENCE CRITERION FOR TWO SUCCESSIVE	AMP00490
C	ITERATIONS OF F.	AMP00500
C	P= THE AVERAGE POWER DISSIPATED BY THE POWER	AMP00510
C	MOSFET IN ONE SWITCHING CYCLE.	AMP00520
C	PI= NUMERICAL CONSTANT OF PI RADIANS.	AMP00530
C	Q= THE AVERAGE AMOUNT OF CHARGE TRANSFERRED BY	AMP00540
C	THE POWER MOSFET DURING SWITCH ON-TIME.	AMP00550
C	X= VECTOR OF LENGTH N CONTAINING: ON INPUT THE	AMP00560
C	INITIAL PARAMETER ESTIMATES AND ON OUTPUT THE	AMP00570
C	FINAL PARAMETER VALUES AS CALCULATED BY ZXMIN.	AMP00580
C	W= A VECTOR OF LENGTH 3*N USED AS A WORKING SPACE.	AMP00590
C	ON OUTPUT, WORK(1), CONTAINS FOR	AMP00600
C	I=1, NORM OF THE GRADIENT	AMP00610
C	I=2, NUMBER OF FUNCTION CALCULATIONS REQUIRED	AMP00620
C	I=3, ESTIMATE OF THE NUMBER OF SIGNIFICANT	AMP00630
C	DIGITS IN THE FINAL PARAMETER ESTIMATES	AMP00640
C	USER MUST SELECT ARRAY SIZES. ARRAY SIZE IS A FUNCTION OF	AMP00650
C	"N" PARAMETER VALUES.	AMP00660
C	EXTERNAL FUNCT	AMP00670
C	INTEGER N, NSIG, MAXFN, IOPT	AMP00680
C	REAL X(2), H(3), G(2), W(6), F, PI	AMP00690
C	REAL X(3), H(6), G(3), W(9), F, PI	AMP00700
C	REAL X(5), H(15), G(5), W(15), F, PI	AMP00710
C	INITIAL CONDITIONS	AMP00720
C	IOPT=0	AMP00730
C	MAXFN=300	AMP00740
C	N=1	AMP00750
C	N=3	AMP00760
C	N=5	AMP00770

```

NSIG=4
PI= 3.141592654

C INITIAL PARAMETER ESTIMATES
C X(1)=TAU1 1.0 =TAU2 X(4)=TAU3
C X(2)=IMAX1 X(3)=IMAX2 X(5)=IMAX3

X(1)= 0.53456789
X(2)= 0.93459999
X(3)= 1.38456789
C X(4)= 0.375
C X(5)= 0.250

CALL ZXMIN(FUNCT,N,NSIG,MAXFN,I0FT,X,H,G,F,W,IER)

C COMPUTE AVERAGE AMOUNT OF CHARGE AND MINIMUM POWER
C DISSIPATED BY SWITCHING ELEMENT OVER PERIOD T FOR EACH
C TYPE OF CURRENT WAVEFORM.

* SINE WAVEFORM
C Q=2.0/PI*(X(1)*X(2))
C P=.5*X(1)*X(2)**2.0
*****

* RAMP WAVEFORM
C Q=.5*X(1)*X(2)
C P=X(1)/3.0*X(2)**2.0
*****

* SINE-SINE WAVEFORM
C Q= (2.0/PI)*(X(1)*X(2) + X(3))
C P= ( (.5*(X(1)*X(2)**2.0 + X(3)**2.0) + (2.0*X(2)*X(3)*X(1)*X(4)) )
C CSIN(PI*X(1))) / (PI*(1.0-X(1)**2.0)))
*****

* RAMP-SINE WAVEFORM
C Q=2.0/PI * (X(1)*X(2) + .25*PI*X(3))
C P= ( ((.5*X(1)*X(2)**2.0) + ((X(3)**2.0)/3.0) + ((2.0*X(2)*
C X(3)*X(1)**2.0)/PI)))
*****

* RAMP-SINE-SINE WAVEFORM
C Q=2.0/PI*(X(1)*X(2) + X(4)*X(5)) + .5*X(3)
C P= ( ((.5*X(1)*X(2)**2.0) + (1.0/3.0*X(3)**2.0) + (.5*X(4)
C *X(5)**2.0) + (SIN(PI*X(1)/X(4)))*(4.0*X(2)*X(5)*X(1)*X(4)**2.0)/
C C(PI*(X(4)**2.0 - X(1)**2.0))) + (2.0/PI*(X(2)*X(3)*X(1)**2.0 +
C CX(3)*X(5)*X(4)**2.0)))
*****

* SINE-SINE-SINE WAVEFORM
C Q= ( ((2.0/PI)*(X(1)*X(2) + X(3) - X(4)*X(5)))
C P= ( (.5*(X(1)*X(2)**2.0 + X(3)**2.0 + X(4)*X(5)**2.0) -

```

```

AMP01130
AMP01140
AMP01150
AMP01160
AMP01170
AMP01180
AMP01190
AMP01200
AMP01210
AMP01220
AMP01230
AMP01240
AMP01250
AMP01260
AMP01270
AMP01280
AMP01290
AMP01300
AMP01310
AMP01320
AMP01330
AMP01340
AMP01350
AMP01360
AMP01370
AMP01380
AMP01390
AMP01400
AMP01410
AMP01420
AMP01430
AMP01440
AMP01450
AMP01460
AMP01470
AMP01480
AMP01490
AMP01500
AMP01510
AMP01520
AMP01530
AMP01540
AMP01550
AMP01560
AMP01570
AMP01580
AMP01590
AMP01600
AMP01610
AMP01620
AMP01630
AMP01640
AMP01650
AMP01660
AMP01670
AMP01680

```

```

C      C4.0/PI*(SIN(PI*X(1)/X(4))*(X(2)*X(5)*X(1)*X(4)**2.0)/(X(4)**2.0)
C      C- X(1)**2.0) + SIN(PI*X(1))*X(2)*X(3)*X(1)/(1.0 - X(1)**2.0) +
C      CSIN(PI*X(4))*X(5)*X(3)*X(4)/(1.0-X(4)**2.0)))
C      *****
C      PRINT ZXMIN FINAL PARAMETER ESTIMATES AND RESULTING VALUES
C      OF IER, Q, P, AND F.
C      PRINT *, 'IER=', IER
C      PRINT *, 'X(1)=', X(1)
C      PRINT *, 'X(2)=', X(2)
C      PRINT *, 'X(3)=', X(3)
C      PRINT *, 'X(4)=', X(4)
C      PRINT *, 'X(5)=', X(5)
C      PRINT *, 'Q=', Q
C      PRINT *, 'P=', P
C      PRINT *, 'F=', F
C      GRAFH NUMERICAL RESULTS
C      CALL S(1.0,X(2))
C      CALL T(1.0,X(2))
C      CALL SS(X(1),1.0,X(2),X(3))
C      CALL TS(X(1),1.0,X(2),X(3))
C      CALL TSS(X(1),1.0,X(2),X(3),X(4),X(5))
C      CALL SSS(X(1),1.0,X(2),X(3),X(4),X(5))
C      STOP
C      END
C      *****
C      SUBROUTINE FUNCT(N,X,F)
C      *      THIS USER SUPPLIED SUBROUTINE CALCULATES THE MINIMUM
C      *      OF FUNCTION F FOR X(I), I=1,...,N GIVEN PARAMETER ESTIMATES.
C      *      USER MUST SELECT APPROPRIATE WAVEFORM COMBINATION PRIOR TO
C      *      EACH PROGRAM RUN.
C      *      *** POWER MINIMIZATION OF WAVE FORMS ***
C      *      VARIABLE LISTING
C      *      F=      SCALAR VALUE OF MINIMIZED FUNCTION AT FINAL
C      *      PARAMETER ESTIMATES.
C      *      N=      THE NUMBER OF PARAMETER VALUES.
C      *      X=      VECTOR OF LENGTH N CONTAINING: ON INPUT THE
C      *      INITIAL PARAMETER ESTIMATES AND ON OUTPUT THE
C      *      FINAL PARAMETER VALUES AS CALCULATED BY ZXMIN.
C      *      X(1)=TAU1  X(2)=INAX1

```

```

*          X(3)=IMAX2
*          X(4)=TAU3  X(5)=IMAX3
      INTEGER N
      REAL X(N),F,Q,P
      REAL PI
      PI= 3.141592654

*      SINE WAVE
C      X(1)=1.0
C      X(2)=.5*PI/X(1)
C      F=ABS(1.0 - (.5*X(1)*X(2)**2.0))
*****

*      RAMP WAVEFORM
C      X(1)=1.0
C      X(2)=1.0/X(1)
C      F=ABS(1.0 - (X(1)/3.0*X(2)**2.0))
*****

*      SINE-SINE WAVEFORM
C      X(1)=PI/2.0 - X(3))/X(2)
C      F=ABS(1.0 - ((.5*X(1)*X(2)**2.0 + X(3)**2.0) + (2.0*X(2)*X(3)*X(1)*
C      CSIN(PI*X(1))) / (PI*(1.0-X(1)**2.0))))
*****

*      RAMP-SINE WAVEFORM
C      X(1)=.5*PI/X(2)*(1.0 - .5*X(3))
C      F=ABS(1.0 - ((.5*X(1)*X(2)**2.0) + ((X(3)**2.0)/3.0) + ((2.0*X(2)*
C      CN(3)*X(1)**2.0)/PI)))
*****

*      RAMP-SINE-SINE WAVEFORM
C      X(2)=.669
C      X(3)=.6616
C      X(1)=1.0
C      X(3)=1.0*(1.0 - 2.0/PI*(X(1)*X(2) + X(4)*X(5)))
C      F=ABS(1.0 - ((.5*X(1)*X(2)**2.0) + (1.0/3.0*X(3)**2.0) + (.5*X(4)
C      C*(X(1)**2.0) + (SIN(PI*X(1)/X(4)))*(4.0*X(2)*X(5)*X(1)*X(4)**2.0)/
C      C(PI*(X(1)**2.0 - X(1)**2.0))) + (2.0/PI*(X(2)*X(3)*X(1)**2.0 +
C      CN(3)*X(5)*X(4)**2.0))))
C      Q=ABS(1.0 - (2.0/PI*(X(1)*X(2) + X(4)*X(5)) + .5*X(3)))
*****

*      SINE-SINE-SINE WAVEFORM
C      X(1)=ABS(X(1))
C      X(2)=ABS(X(2))
C      X(4)=ABS(X(4))
C      X(5)=ABS(X(5))
C      IF(X(1).LT.1.01)GO TO 42
C      X(1)=1.0
C2  IF(X(4).LT.1.01)GO TO 44
C      X(4)=1.0
C      X(3)=.5*PI - X(1)*X(2) - X(4)*X(5)
C4  X(3)=ABS(X(3))

```

```

AMP02250
AMP02260
AMP02270
AMP02280
AMP02290
AMP02300
AMP02310
AMP02320
AMP02330
AMP02340
AMP02350
AMP02360
AMP02370
AMP02380
AMP02390
AMP02400
AMP02410
AMP02420
AMP02430
AMP02440
AMP02450
AMP02460
AMP02470
AMP02480
AMP02490
AMP02500
AMP02510
AMP02520
AMP02530
AMP02540
AMP02550
AMP02560
AMP02570
AMP02580
AMP02590
AMP02600
AMP02610
AMP02620
AMP02630
AMP02640
AMP02650
AMP02660
AMP02670
AMP02680
AMP02690
AMP02700
AMP02710
AMP02720
AMP02730
AMP02740
AMP02750
AMP02760
AMP02770
AMP02780
AMP02790
AMP02800

```

```

C      X(3)=1.35
C      X(4)=.400
C      X(5)=.30
C      X(1)=(.5*PI - X(4)*X(5) - X(3))/X(2)

C      F=ABS(1.0 - (.5*(X(1)*X(2)**2.0 + X(3)**2.0 + X(4)*X(5)**2.0) +
C      C4.0/PI*(SIN(PI*X(1)/X(4))*(X(2)*X(5)*X(1)*X(4)**2.0)/(X(4)**2.0
C      C- X(1)**2.0) + SIN(PI*X(1))*X(2)*X(3)*X(1)/(1.0 - X(1)**2.0) +
C      CSIN(PI*X(4))*X(5)*X(3)*X(4)/(1.0-X(4)**2.0)))

C      F=ABS(1.0 - ((2.0/PI)*((X(1)*X(2)) + X(3) + X(4)*X(5))))
C      F=Q+P
*****
*****
      PRINT *, 'SUBF=',F
      RETURN
      END

*****
*****
      SUBROUTINE S(TAU1,I1MAX)
*      THIS SUBROUTINE PLOTS THE HALF PERIOD OF A SINUSOID.
*
*      ***** VARIABLE LISTING *****
*
*      I1(J)= VALUE OF CURRENT AS A FUNCTION OF TIME.
*      I1MAX= MAXIMUM CURRENT AMPLITUDE OF SINUSOID.
*      J= NUMBER OF POINTS PLOTTED.
*      TAU(J)= ABSCISSA VALUE OF SWITCH ON-TIME.
*      TAU1= HALF PERIOD OF SINUSOID OR SWITCH ON-TIME.
*      T1= FULL PERIOD OF SINUSOID.

      INTEGER J
      REAL TAU1,I1MAX
      REAL T1,I1(100),TAU(100),PI
      OPEN (UNIT=4, FILE='SAMP', STATUS='NEW')

      PI= 3.141592654
      T1=2.0 * TAU1
      DO 10 J=1,100
          I1(J)=I1MAX * SIN((2.0*PI*J)/(T1*100))
          TAU(J)= J/100.0
          WRITE(4,200)TAU(J),I1(J)
          FORMAT(' ',F6.3,BX,F10.7)
200
10      CONTINUE
      RETURN
      END
*****
*****

```



```

SUBROUTINE T(TAU1,I1MAX)
THIS SUBROUTINE PLOTS HALF PERIOD OF A RAMP FUNCTION.

***** VARIABLE LISTING *****

I1(J)= VALUE OF CURRENT AS A FUNCTION OF TIME.
I1MAX= MAXIMUM CURRENT AMPLITUDE OF RAMP.
J= NUMBER OF POINTS PLOTTED.
TAU(J)= ABSCISSA VALUE OF SWITCH ON-TIME.
TAU1= DURATION OF SWITCH ON-TIME.

INTEGER J
REAL TAU1,I1MAX
REAL I1(100),TAU(100),PI
OPEN (UNIT=3, FILE='RAMP', STATUS='NEW')

PI= 3.141592654
DO 10 J=1,100
    TAU(J)=J/100.00
    I1(J)=(I1MAX/TAU1) * TAU(J)
    WRITE(3,200)TAU(J),I1(J)
200    FORMAT(' ',F6.3,3X,F10.7)

10    CONTINUE
    RETURN
    END

*****
SUBROUTINE SS(TAU1,TAU2,I1MAX,I2MAX)
THIS SUBROUTINE PLOTS THE HALF PERIODS OF TWO SINUSOIDS AND THEIR
SUM.

***** VARIABLE LISTING *****

I1(J)= VALUE OF CURRENT AS A FUNCTION OF TIME.
I2(J)= VALUE OF CURRENT AS A FUNCTION OF TIME.
ISUM(J)= SUM OF I1(J) AND I2(J) AS A FUNCTION OF TIME.
I1MAX= MAXIMUM CURRENT AMPLITUDE OF SINUSOID.
I2MAX= MAXIMUM CURRENT AMPLITUDE OF SINUSOID.
J= NUMBER OF POINTS PLOTTED.
TAU(J)= ABSCISSA VALUE OF SWITCH ON-TIME.
TAU1= HALF PERIOD OF SINUSOID.
TAU2= DURATION OF SWITCH ON-TIME.
T1= FULL PERIOD OF SINUSOID TAU1.
T2= FULL PERIOD OF SINUSOID TAU2.

INTEGER J
REAL TAU1,TAU2,I1MAX,I2MAX
REAL T1,T2,I1(100),I2(100),ISUM(100),TAU(100),PI
OPEN (UNIT=6, FILE='SSAMP', STATUS='NEW')

PI= 3.141592654

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AMP03370
 AMP03380
 AMP03390
 AMP03400
 AMP03410
 AMP03420
 AMP03430
 AMP03440
 AMP03450
 AMP03460
 AMP03470
 AMP03480
 AMP03490
 AMP03500
 AMP03510
 AMP03520
 AMP03530
 AMP03540
 AMP03550
 AMP03560
 AMP03570
 AMP03580
 AMP03590
 AMP03600
 AMP03610
 AMP03620
 AMP03630
 AMP03640
 AMP03650
 AMP03660
 AMP03670
 AMP03680
 AMP03690
 AMP03700
 AMP03710
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 AMP03770
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 AMP03790
 AMP03800
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 AMP03820
 AMP03830
 AMP03840
 AMP03850
 AMP03860
 AMP03870
 AMP03880
 AMP03890
 AMP03900
 AMP03910
 AMP03920

```

T1=2.0 * TAU1
T2=2.0 * TAU2
DO 10 J=1,100
    I2(J)=I2MAX * SIN((2.0*PI*J)/(T2*100))
    I1(J)=I1MAX * SIN((2.0*PI*J)/(T1*100))
    TAU(J)= J/100.0
    IF(TAU(J).LT.TAU1)GO TO 13
    IF(I1(J-1).EQ.0)GO TO 14
    IF(I1(J).GT.0)GO TO 15
    I1(J)=0.0
    ISUM(J)= I1(J) + I2(J)
    WRITE(6,200)TAU(J),I1(J),I2(J),ISUM(J)
    FORMAT(' ',F6.3,3X,F10.7,3X,F10.7,3X,F10.7)
10  CONTINUE
    RETURN
    END
*****
*****
*****
SUBROUTINE SSS(TAU1,TAU2,I1MAX,I2MAX,TAU3,I3MAX)
*   THIS SUBROUTINE PLOTS THE HALF PERIODS OF THREE SINUSOIDS AND
*   THEIR SUM.
*
*   ***** VARIABLE LISTING *****
*
*   I1(J)=  VALUE OF CURRENT AS A FUNCTION OF TIME.
*   I2(J)=  VALUE OF CURRENT AS A FUNCTION OF TIME.
*   I3(J)=  VALUE OF CURRENT AS A FUNCTION OF TIME.
*   ISUM(J)= SUM OF I1(J),I2(J),AND I3(J), AS A FUNCTION OF TIME.
*   I1MAX=  MAXIMUM CURRENT AMPLITUDE OF SINUSOID.
*   I2MAX=  MAXIMUM CURRENT AMPLITUDE OF SINUSOID.
*   I3MAX=  MAXIMUM CURRENT AMPLITUDE OF SINUSOID.
*   J=      NUMBER OF POINTS PLOTTED.
*   TAU(J)= ABSOISSA VALUE OF SWITCH ON-TIME.
*   TAU1=   HALF PERIOD OF SINUSOID.
*   TAU2=   DURATION OF SWITCH ON-TIME.
*   TAU3=   HALF PERIOD OF SINUSOID.
*   T1=     FULL PERIOD OF SINUSOID TAU1.
*   T2=     FULL PERIOD OF SINUSOID TAU2.
*   T3=     FULL PERIOD OF SINUSOID TAU3.
*
*
*   INTEGER J
*   REAL TAU1,TAU2,I1MAX,I2MAX,TAU3,I3MAX
*   REAL T1,T2,T3,I1(100),I2(100),I3(100),ISUM(100),TAU(100),PI
*   OPEN (UNIT=7, FILE='SSSAMP', STATUS='NEW')
*
*   PI= 3.141592654
*   T1=2.0 * TAU1
*   T2=2.0 * TAU2
*   T3=2.0 * TAU3

```

```

DO 10 J=1,100
    I3(J)=I3MAX * SIN((2.0*PI*J)/(T3*100))
    I2(J)=I2MAX * SIN((2.0*PI*J)/(T2*100))
    I1(J)=I1MAX * SIN((2.0*PI*J)/(T1*100))
    TAU(J)=J/100.00
    IF(TAU(J).LT.TAU1)GO TO 13
    I1(J)=0.0
13    IF(TAU(J).LT.TAU3)GO TO 15
    I3(J)=0.0
15    ISUM(J)= I1(J) + I2(J) + I3(J)
    WRITE(7,200)TAU(J),I1(J),I2(J),I3(J),ISUM(J)
200    FORMAT(' ',F6.3,3X,F10.7,3X,F10.7,3X,F10.7,3X,F10.7)
10    CONTINUE
    RETURN
END

```

***** VARIABLE LISTING *****

```

*      I1(J)=  VALUE OF SINUSOIDAL CURRENT AS A FUNCTION OF TIME.
*      I2(J)=  VALUE OF RAMP CURRENT AS A FUNCTION OF TIME.
*      ISUM(J)= SUM OF I1(J) AND I2(J) AS A FUNCTION OF TIME.
*      I1MAX=  MAXIMUM CURRENT AMPLITUDE OF SINUSOID.
*      I2MAX=  MAXIMUM CURRENT AMPLITUDE OF RAMP.
*      J=      NUMBER OF POINTS PLOTTED.
*      TAU(J)=  ABSCISSA VALUE OF SWITCH ON-TIME.
*      TAU1=   HALF PERIOD OF SINUSOID.
*      TAU1=   DURATION OF SWITCH ON-TIME.
*      T1=     FULL PERIOD OF SINUSOID TAU1.

```

```

REAL TAU1,TAU2,I1MAX,I2MAX
REAL T1,I1(100),I2(100),ISUM(100),TAU(100),PI
INTEGER J
OPEN (UNIT=1, FILE='STAMP', STATUS='NEW')

PI= 3.141592654
T1=0.0 * TAU1
DO 10 J=1,100
    TAU(J)=J/100.00
    I1(J)=I1MAX * SIN((2.0*PI*J)/(T1*100))
    I2(J)= (I2MAX/TAU1) * TAU(J)
    IF(TAU(J).LT.TAU1)GO TO 13
    I1(J)=0.0
13    ISUM(J)= I1(J) + I2(J)
    WRITE(1,200)TAU(J),I1(J),I2(J),ISUM(J)
200    FORMAT(' ',F6.3,3X,F10.7,3X,F10.7,3X,F10.7)
10    CONTINUE
    RETURN

```

```

END
SUBROUTINE TSS(TAU1,TAU2,I1MAX,I2MAX,TAU3,I3MAX)
C THIS SUBROUTINE PLOTS THE HALF PERIODS OF TWO SINUSOIDS, A RAMP
* FUNCTION, AND THEIR SUM.
**
**      *** VARIABLE LISTING ***
**
**      I1(J)=   VALUE OF SINUSOIDAL CURRENT AS A FUNCTION OF TIME.
**      I2(J)=   VALUE OF RAMP CURRENT AS A FUNCTION OF TIME.
**      I3(J)=   VALUE OF SINUSOIDAL CURRENT AS A FUNCTION OF TIME.
**      ISUM(J)=  SUM OF I1(J),I2(J),AND I3(J), AS A FUNCTION OF TIME.
**      I1MAX=    MAXIMUM CURRENT AMPLITUDE OF SINUSOID.
**      I2MAX=    MAXIMUM CURRENT AMPLITUDE OF RAMP.
**      I3MAX=    MAXIMUM CURRENT AMPLITUDE OF SINUSOID.
**      J=        NUMBER OF POINTS PLOTTED.
**      TAU1(J)=  ABSCISSA VALUE OF SWITCH ON-TIME.
**      TAU1=     HALF PERIOD OF SINUSOID.
**      TAU2=     DURATION OF SWITCH ON-TIME.
**      TAU3=     HALF PERIOD OF SINUSOID.
**      T1=       FULL PERIOD OF SINUSOID TAU1.
**      T3=       FULL PERIOD OF SINUSOID TAU3.
**
INTEGER J
REAL TAU1,TAU2,I1MAX,I2MAX,TAU3,I3MAX
REAL T1,T3,I1(100),I2(100),I3(100),ISUM(100),TAU(100),PI
OPEN (UNIT=9, FILE='TSSAMP', STATUS='NEW')
PI= 3.141592654
T1=2.0 * TAU1
T3=2.0 * TAU3
DO 10 J=1,100
  TAU(J)=J/100.00
  I1(J)=I1MAX * SIN((2.0*PI*J)/((T1*100)))
  I2(J)=(I2MAX/TAU2) * TAU(J)
  I3(J)=I3MAX * SIN((2.0*PI*J)/((T3*100)))
  ISUM(J)=I1(J)+I2(J)+I3(J)
  IF(TAU(J).LT.TAU1)GO TO 13
  IF(J)=0.0
13  IF(TAU(J).LT.TAU3)GO TO 15
  I3(J)=0.0
15  ISUM(J) = I1(J) + I2(J) + I3(J)
WRITE(9,100)TAU(J),I1(J),I2(J),I3(J),ISUM(J)
FORMAT(' ',F6.3,3X,F10.7,3X,F10.7,3X,F10.7,3X,F10.7)
100 CONTINUE
RETURN
END

```

AMP0550

SUBF=	0.0852299
SUBF=	0.0852299
SUBF=	0.0852356
SUBF=	0.0852289
SUBF=	0.0852013
SUBF=	0.0851917
SUBF=	0.0851917
SUBF=	0.0851917
SUBF=	0.0851889
SUBF=	0.0851879
SUBF=	0.0851889
SUBF=	0.0851879
SUBF=	0.0851879
SUBF=	0.0851879
SUBF=	0.0851879
SUBF=	0.0851879
SUBF=	0.0851889
SUBF=	0.0851879
SUBF=	0.0851898
SUBF=	0.0851879
SUBF=	0.0851879
SUBF=	0.0851879

*** TERMINAL ERROR (IER = 130) FROM IMSL ROUTINE ZXMIN

IER=	130
N(1)=	0.5227677
N(2)=	0.9210671
N(3)=	1.3882856
Q=	1.0006771
P=	1.0866613
F=	0.0851879 0

Compile time (seconds): 0.13 Execution time (seconds): 0.92

APPENDIX B: 14 V, 14 W, BUCK/ZCS QUASI-RESONANT BUCK DC-DC CONVERTER

PARTS LIST

Switching Transistor

BUZ 60 8627 N-channel Enhancement Mode Transistor, 400 V, 1 Ω , 5.5 Amps

Inductors

L_r - 21.4 μ H, Core 55208-A2 ($\mu = 26$), 22 turns of 22 AWG

L_0 - 15.35 mH, Core FD78HL237350, $\frac{1}{2}$ Amp

L - 51.3 μ H, Core 55208-A2 ($\mu = 26$), 53 turns of 24 AWG

Capacitors

$$C_r = C_1 + C_2 + C_3 + C_4 = 48.8 \times 10^{-9} F$$

C_1 - 20.1 nF, 100 V, Z5U

C_2 - 14.07 nF, 100 V, Z5U

C_3 - AE, 9.8 nF, 1 kV

C_4 - 438804 Gudeman XFS-1813-10, 4.83 nF, 600 VDC

$$C = C_5 + C_6 + C_7 = 1.21 \text{ mF}$$

C_5 - USI, 594 μ F, 50 V

C_6 - USI, 514 μ F, 50 V

C_7 - Sprauge, 96.7 μ F, TE-1210, 75-25 DC, USA 7430 H

Diodes

D_1 - MUR 410 Ultrafast Rectifier, VR = 100 V, $I_{F(AV)} = 4$ Amps

D_2 - MUR 410 Ultrafast Rectifier, VR = 100 V, $I_{F(AV)} = 4$ Amps

D_3 - MBR 735 Schottky Barrier Rectifier, $V_R = 35 \text{ V}$, $I_{F(AV)} = 7.5 \text{ Amps}$

D_4 - MBR 735 Schottky Barrier Rectifier, $V_R = 35 \text{ V}$, $I_{F(AV)} = 7.5 \text{ Amps}$

Resistors

R_{LOAD} - Jagabi Lubri-tact Rheostat, 53Ω , 3 Amps

R_G - 10.19Ω

Support Equipment

Power Designs Inc. Regulated DC Power Supply, 0-36 V, 0 ~ 5 Amps

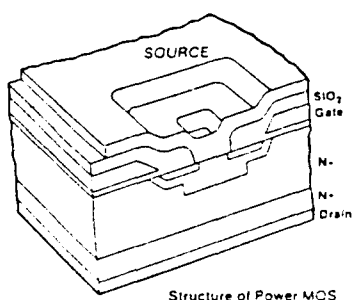
APPENDIX C: SWITCHING ELEMENT DATA

POWERMOS TRANSISTORS QUICK SELECTION CHART [From Ref. 38]

POWERMOS TRANSISTORS

This broad range of N-Channel enhancement mode MOSFET's facilitates simpler, faster power control in a wide variety of application. They can be driven from microcomputers and TTL, and have a switching speed that is several times faster than conventional bipolar devices.

Types are available with drain-source voltage ratings up to 1000V. All are manufactured to have a controlled threshold voltage, and all exhibit low on-resistance and high transconductance.



TO-3



TO-220AB

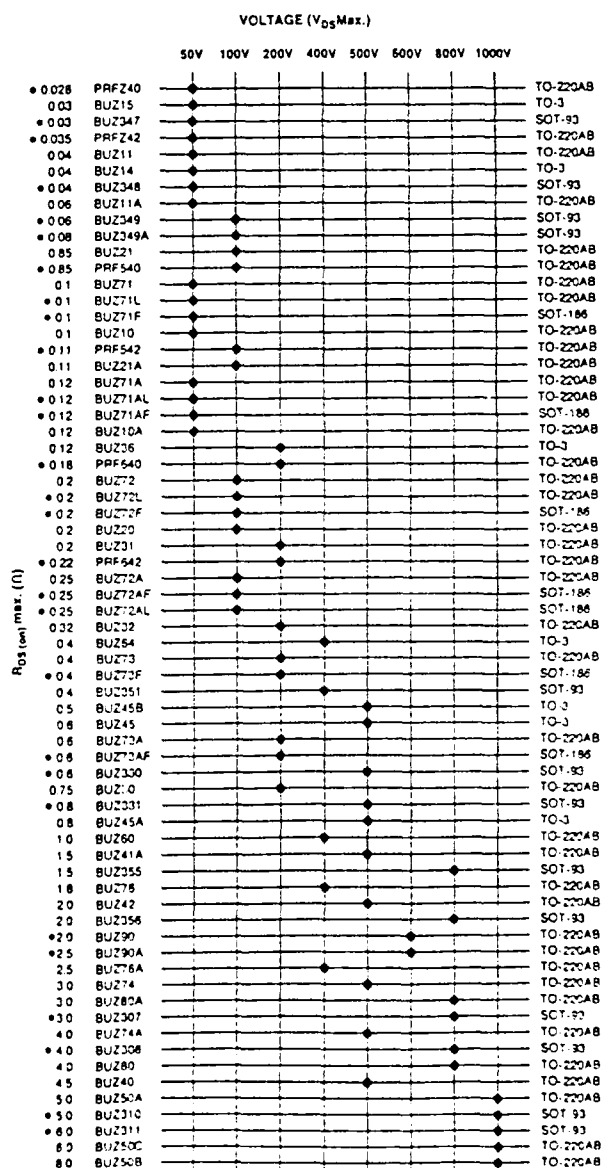


SOT-93



SOT-186

QUICK SELECTION CHART

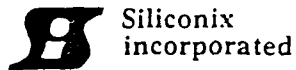


• NEW FOR '88!

BASIC DATA (in order of voltage/package/current)							
Vos max. V	Type Number	Package Outline	I _p max. A	P _{tot} max. W	R _{DS ON} < Ω	g _{fs} typ. A/V	C _{iss} typ. pF
50	BUZ10	TO-220AB	12	75	0.1	4.8	120
	BUZ10A		12	75	0.12	4.8	120
	BUZ71		12	40	0.1	4.8	160
	BUZ71L		12	40	0.1	4.8	160
	BUZ71A		12	40	0.12	4.8	160
	BUZ71AL		12	40	0.12	4.8	160
	BUZ11A		25	75	0.06	8.0	360
	BUZ11		30	75	0.04	8.0	360
	PRFZ42		46	125	0.035	22	250
	PRFZ40		51	125	0.028	22	250
50	BUZ14	TO-3	39	125	0.04	12.0	500
	BUZ15		45	125	0.03	12.0	500
50	BUZ348	SOT-93	43	125	0.04	18	800
	BUZ347		49	125	0.03	18	800
50	BUZ71AF	SOT-186	11	40	0.12	4.8	160
	BUZ71F		12	40	0.1	4.8	160
100	BUZ72A	TO-220AB	11	40	0.25	3.8	80
	BUZ72AL		11	40	0.25	3.8	80
	BUZ20		12	75	0.2	4.0	80
	BUZ72		12.5	40	0.2	3.8	80
	BUZ72L		12.5	40	0.2	3.8	80
	BUZ21A		21	75	0.11	3.5	200
	BUZ21		24	75	0.1	3.5	200
	PRF542		24	150	0.1	13	90
	PRF540		27	150	0.085	13	90
100	BUZ349A	SOT-93	28	125	0.08	18	500
	BUZ349		32	125	0.06	18	500
100	BUZ72AF	SOT-186	7	40	0.25	3.8	80
	BUZ72F		8	40	0.2	3.8	80
200	BUZ73A	TO-220AB	5.8	40	0.6	3.5	80
	BUZ73		7	40	0.4	3.5	80
	BUZ30		7	75	0.75	3.5	100
	BUZ32		9.5	75	0.4	3.5	100
	BUZ31		12.5	75	0.2	5.0	140
	PRF642		16	125	0.22	10	93
	PRF640		18	125	0.18	10	93
200	BUZ35	TO-3	22	125	0.12	7.5	500
200	BUZ73AF	SOT-186	4.3	40	0.6	3.5	80
	BUZ73F		5.3	40	0.4	3.5	80
400	BUZ75A	TO-220AB	2.6	40	2.5	2.5	25
	BUZ75		3	40	1.8	2.5	25
	BUZ60		5.5	75	1.0	1.5	30
400	BUZ64	TO-3	10.5	125	0.4	4.5	100
400	BUZ351	SOT-93	11.5	125	0.4	4.5	100
500	BUZ74A	TO-220AB	2.0	40	4.0	2.5	20
	BUZ74		2.4	40	3.0	2.5	20
	BUZ40		2.5	75	4.5	2.5	30
	BUZ42		4.0	75	2.0	2.5	30
	BUZ41A		4.5	75	1.5	2.5	30
500	BUZ45A	TO-3	8.3	125	0.8	4.0	100
	BUZ45		9.6	125	0.6	4.0	100
	BUZ45B		10	125	0.5	4.0	100
500	BUZ331	SOT-93	8.0	125	0.8	8.0	120
	BUZ330		9.5	125	0.6	8.0	120
600	BUZ90A	TO-220AB	3.5	75	2.5	2.5	70
	BUZ90		4.0	75	2.0	2.5	70
800	BUZ80	TO-220AB	2.6	75	4.0	1.8	30
	BUZ80A		3.0	75	3.0	1.8	30
800	BUZ307	SOT-93	3.0	75	3.0	1.8	55
	BUZ308		4.0	75	4.0	1.8	55
	BUZ355		6	125	1.5	1.8	140
	BUZ356		5	125	2.0	1.8	140
1000	BUZ50B	TO-220AB	2.0	75	8.0	1.5	30
	BUZ50C		2.25	75	6.0	1.5	30
	BUZ50A		2.5	75	5.0	1.5	30
1000	BUZ311	SOT-93	2.3	75	6.0	1.5	55
	BUZ310		2.5	75	5.0	1.5	55

BUZ60 N-CHANNEL ENHANCEMENT MODE TRANSISTOR

DATA SHEET [From Ref. 48]



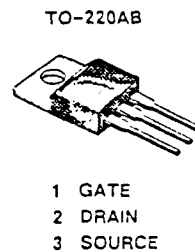
MOSPOWER

BUZ60

N-Channel Enhancement Mode Transistor

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
BUZ60	400	1.0	5.5



TOP VIEW



ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	BUZ60	Units
Drain-Source Voltage	V_{DS}	400	V
Gate-Source Voltage	V_{GS}	± 40	
Continuous Drain Current	I_D	5.5	A
		3.7	
Pulsed Drain Current ¹	I_{DM}	22	A
Avalanche Current (see figure 9)	I_A	5.5	
Power Dissipation	P_D	75	W
		30	
Operating Junction & Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Lead Temperature (1/16" from case for 10 secs.)	T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.57	K°W
Junction-to-Ambient	R_{thJA}	-	75	
Case-to-Sink	R_{thCS}	1	-	

¹Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage $V_{GS} = 0, I_D = 250 \mu\text{A}$		$V_{(BR)DSS}$	400	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}, I_D = 1000 \mu\text{A}$		$V_{GS(th)}$	2.1	-	4.0	
Gate-Body Leakage $V_{DS} = 0, V_{GS} = \pm 20 \text{ V}$		I_{GSS}	-	10	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}, V_{GS} = 0$		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}, V_{GS} = 0, T_J = 125^\circ\text{C}$		I_{DSS}	-	-	1000	
On-State Drain Current ² $V_{DS} = 10 \text{ V}, V_{GS} = 10 \text{ V}$		$I_{D(on)}$	5.5	-	-	A
Drain-Source On-State Resistance ² $V_{GS} = 10 \text{ V}, I_D = 2.5 \text{ A}$		$r_{DS(on)}$	-	0.8	1.0	Ω
Drain-Source On-State Resistance ² $V_{GS} = 10 \text{ V}, I_D = 2.5 \text{ A}, T_J = 125^\circ\text{C}$		$r_{DS(on)}$	-	1.5	1.9	
Forward Transconductance ² $V_{DS} = 15 \text{ V}, I_D = 2.5 \text{ A}$		g_{fs}	1.7	2.2	-	S(V)
Input Capacitance	$V_{GS} = 0$ $V_{DS} = 25 \text{ V}$ $f = 1 \text{ MHz}$	C_{iss}	-	750	2000	pF
Output Capacitance		C_{oss}	-	150	180	
Reverse Transfer Capacitance		C_{rss}	-	50	60	
Total Gate Charge	$V_{DS} = 0.5 \times V_{(BR)DSS}$ $V_{GS} = 10 \text{ V}, I_D = 5.5 \text{ A}$ (Gate charge is essentially independent of operating temperature)	Q_g	-	23	30	nC
Gate-Source Charge		Q_{gs}	-	7	-	
Gate-Drain Charge		Q_{gd}	-	12	-	
Turn-On Delay Time	$V_{DD} = 30 \text{ V}, R_L = 10 \Omega$ $I_D = 2.7 \text{ A}, V_{GEN} = 10 \text{ V}$ $R_G = 25 \Omega$ (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	22	45	ns
Rise Time		t_r	-	45	60	
Turn-Off Delay Time		$t_{d(off)}$	-	80	140	
Fall Time		t_f	-	55	65	

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	5.5	A
Pulsed Current ¹	I_{SM}	-	-	22	
Forward Voltage ² $I_F = 2 \times I_S, V_{GS} = 0$	V_{SD}	-	1.2	1.6	V
Reverse Recovery Time $I_F = I_S, dI_F/dt = 100 \text{ A}/\mu\text{s}$	t_{rr}	-	250	-	ns
Reverse Recovered Charge $I_F = I_S, dI_F/dt = 100 \text{ A}/\mu\text{s}$	Q_{rr}	-	1.5	-	μC

¹ Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)² Pulse test: Pulse width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

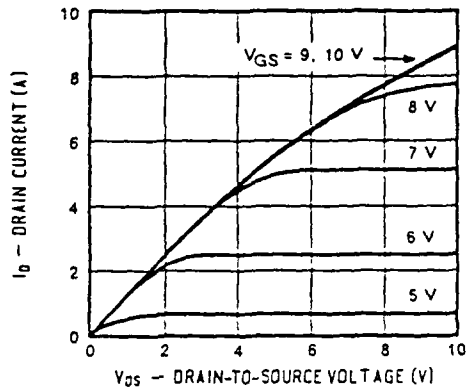


FIGURE 2: Typical Transfer Characteristics

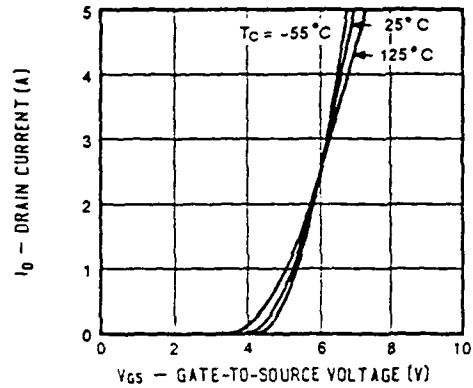


FIGURE 3: Typical Transconductance

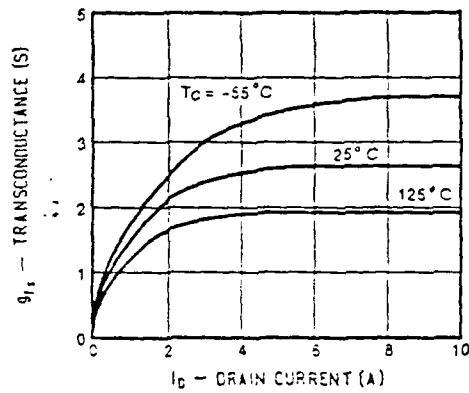


FIGURE 4: Typical On-Resistance

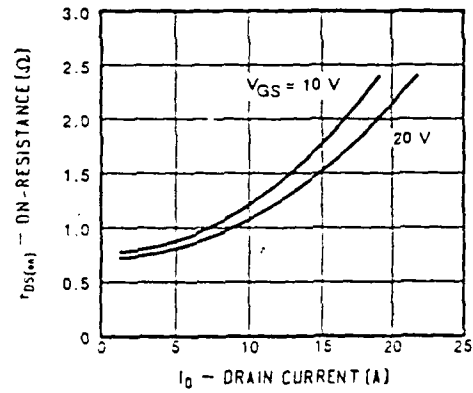


FIGURE 5: Typical Capacitance

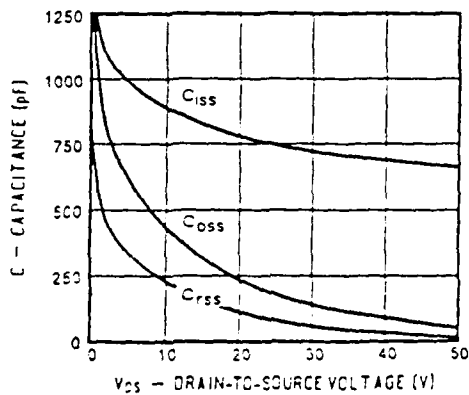
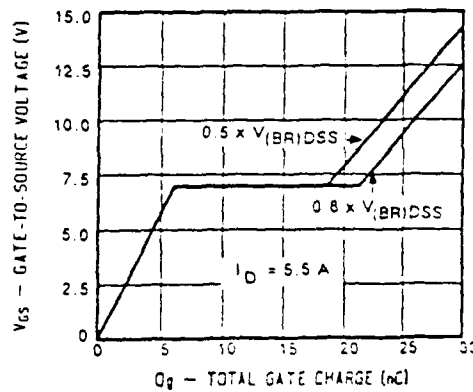


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

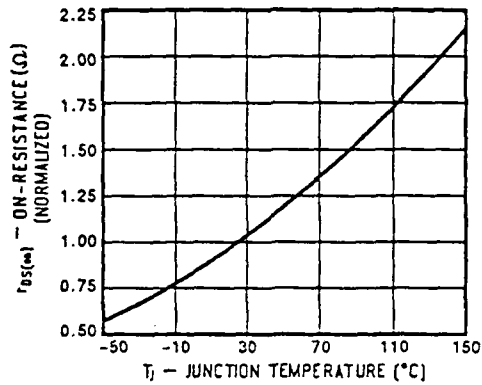


FIGURE 8: Typical Source-Drain Diode Forward Voltage

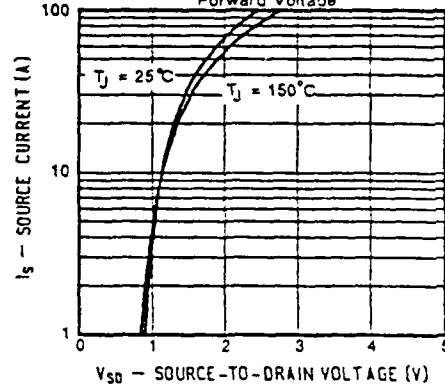


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

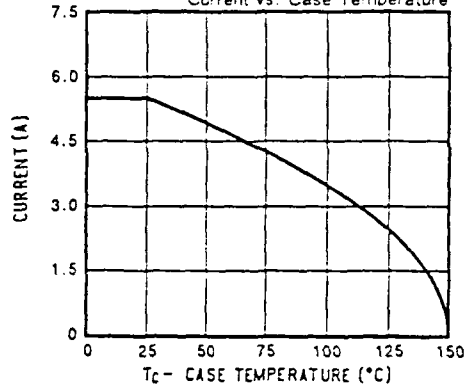


FIGURE 10: Safe Operating Area

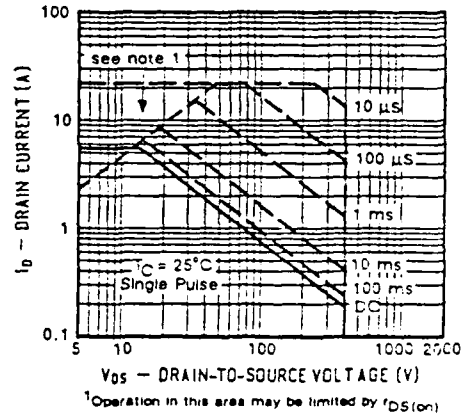
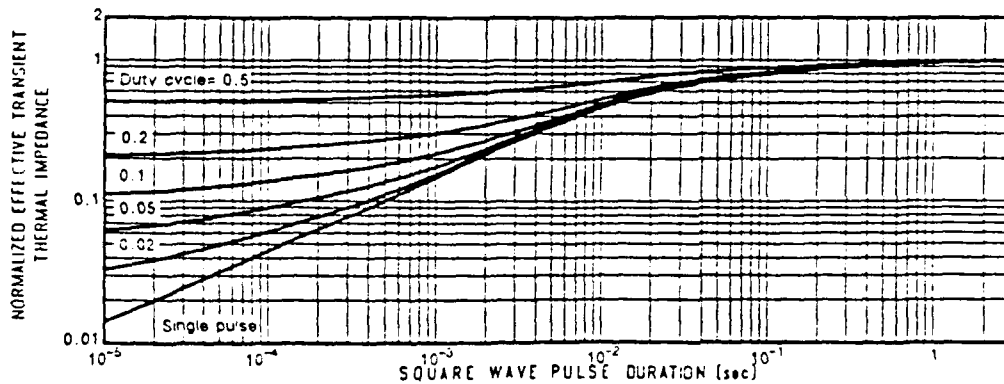


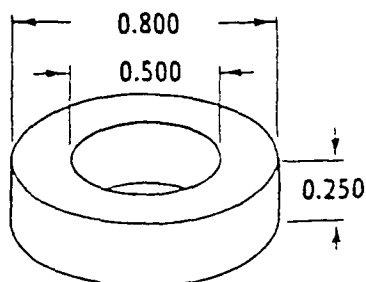
FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



APPENDIX D: GENERAL SWITCH-MODE POWER CONVERSION STORAGE COMPONENTS AND SWITCHES

INDUCTOR CORE MAGNETIC AND WINDING INFORMATION

DATA SHEET [From Ref. 49]



WINDOW AREA	225.600	cm ²
CROSS SECTION	0.0350	in ²
PATH LENGTH	2.01	in
WEIGHT	0.36	oz
	(0.023 lb)	

WINDING TURN LENGTH

WINDING FACTOR	LENGTH/TURN
100% (UNITY)	0.1204 ft 3.67 cm
60%	0.1032 ft 3.15 cm
40%	0.0864 ft 2.64 cm
20%	0.0791 ft 2.41 cm
0%	0.0763 ft 2.33 cm

CORE DIMENSIONS AFTER FINISH

OD (MAX.)	0.830 in	21.1 mm
ID (MIN.)	0.475 in	12.07 mm
HT (MAX.)	0.280 in	7.11 mm

WOUND COIL DIMENSIONS

UNITY WINDING FACTOR

OD (MAX.)	1.148 in	29.2 mm
HT (MAX.)	0.684 in	17.4 mm

MAGNETIC INFORMATION

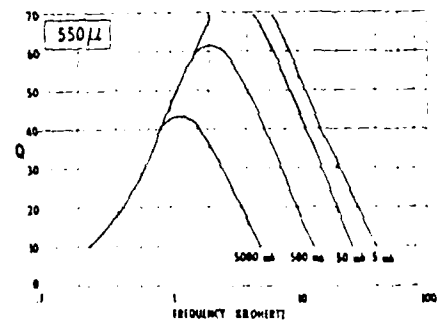
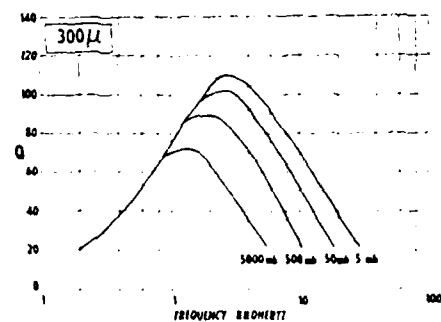
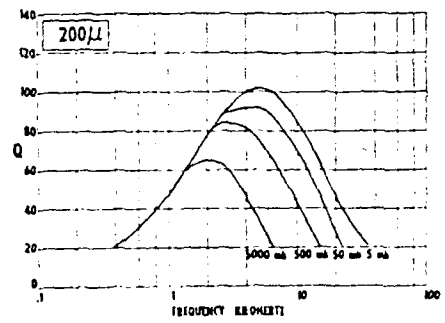
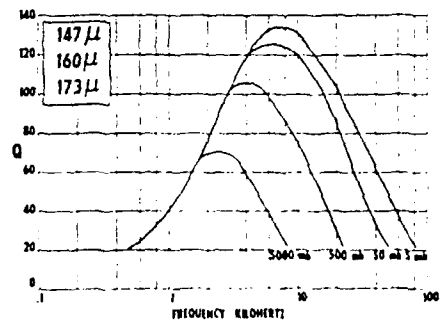
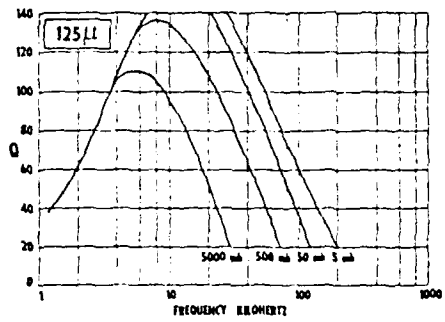
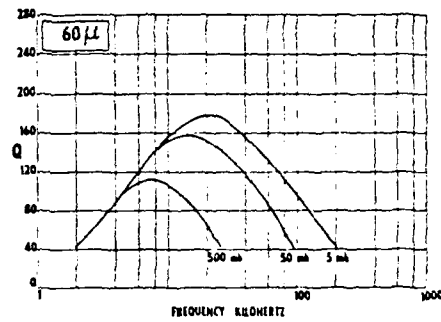
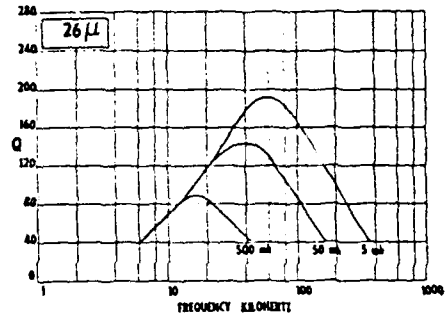
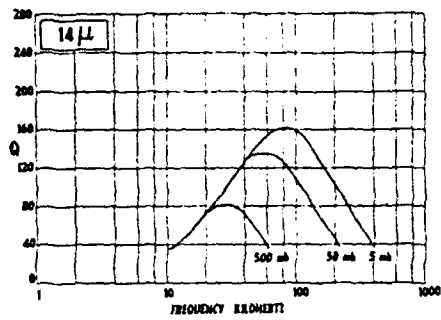
PART NO.	PERM.	INDUCTANCE @ 1000 TURNS	NOMINAL DC RESISTANCE	FINISHES AND STABILIZATIONS	GRADING STATUS	B/NIT GAUSS PER AMP-TURN
55209-	14	7.8	1.03	A2	*	3.46 (<1500 gauss)
55208-	26	14	0.573	A2	*	6.42 (<1500 gauss)
55848-	60	32	0.251	ALL	YES	14.8 (<1500 gauss)
55206-	125	68	0.118	ALL	YES	30.9 (<1500 gauss)
55235-	147	81	0.0990	ALL	YES	36.3 (<1500 gauss)
55204-	160	87	0.0922	ALL	YES	39.5 (<1500 gauss)
55200-	173	95	0.0835	ALL	YES	42.7 (<1500 gauss)
55203-	200	109	0.0736	ALL	YES	49.4 (<600 gauss)
55201-	300	163	0.0492	A2 and L6	YES	74.1 (<300 gauss)
55202-	550	320	0.0250	A2	YES	136 (<50 gauss)

14, 26, 60 and 125 μ
types are available
as high flux cores.
See p. 84, "How to Order".

WINDING INFORMATION FOR UNITY WINDING FACTOR**

AWG			Rdc	AWG			Rdc
WIRE SIZE	TURNS	OHMS		WIRE SIZE	TURNS	OHMS	
11	25	0.00374		26	664	3.28	
12	31	0.00591		27	836	5.17	
13	39	0.00929		28	1.025	8.06	
14	48	0.01463		29	1.253	12.41	
15	60	0.0230		30	1.567	19.62	
16	75	0.0364		31	1.928	30.4	
17	93	0.0567		32	2.350	45.8	
18	116	0.0895		33	2.915	72.3	
19	145	0.1402		34	3.711	116.6	
20	181	0.220		35	4.605	183.5	
21	226	0.348		36	5.683	284	
22	279	0.543		37	6.942	429	
23	347	0.848		38	8.578	677	
24	430	1.330		39	11.170	1,139	
25	531	2.07		40	14.102	1,823	

NOTES: *PLEASE CHECK WITH FIELD SALES OFFICE FOR FURTHER STABILIZATION AND GRADING INFORMATION.
**THE NOMINAL DC RESISTANCE AND THE RDC ARE THEORETICAL VALUES NOT ATTAINABLE IN PRACTICE.
PLEASE SEE WINDING CONSIDERATIONS.



SWITCHMODE POWER RECTIFIERS DATA SHEET [From Ref. 50]

1. Schottky Barrier [From Ref. 50]

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MBR320P MBR330P
MBR340P
See Page 3-50

SWITCHMODE POWER RECTIFIERS

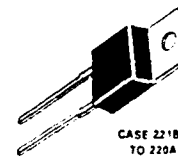
using the Schottky Barrier principle with a platinum barrier metal.
These state-of-the-art devices have the following features:

- Guardring for Stress Protection
- Low Forward Voltage
- 150°C Operating Junction Temperature
- Guaranteed Reverse Avalanche
- Epoxy Meets UL94 VO at 1-8"

MBR735
MBR745

SCHOTTKY BARRIER
RECTIFIERS

7.5 AMPERES
35 and 45 VOLTS



CASE 2218 C1
TO 220AC
PLASTIC

MAXIMUM RATINGS

Rating	Symbol	MBR735	MBR745	Unit
Peak Repetitive Reverse Voltage	V_{RRM}	35	45	Volts
Working Peak Reverse Voltage	V_{RWM}			
DC Blocking Voltage	V_{BO}			
Average Rectified Forward Current (Rated val.) Tc 105°C	I_{FAV}	7.5	7.5	Amps
Peak Repetitive Forward Current (Rated Val. Square Wave, 20 kHz, Tc 105°C)	I_{FRM}	15	15	Amps
Nonrepetitive Peak Surge Current (Surge applied at rated load conditions halfwave single phase 60 Hz)	I_{FSM}	150	150	Amps
Peak Repetitive Reverse Surge Current (20 us, 10 kHz)	I_{RRM}	10	10	Amps
Operating Junction Temperature	T_J	65 to 150	65 to 150	°C
Storage Temperature	T_{stg}	55 to 175	55 to 175	°C
Voltage Rate of Change (Rated val.)	dV/dt	1000	1000	V/us
THERMAL CHARACTERISTICS				
Maximum Thermal Resistance Junction to Case	$R_{\theta JC}$	30	30	°C/W
Maximum Thermal Resistance Junction to Ambient	$R_{\theta JA}$	60	60	°C/W
ELECTRICAL CHARACTERISTICS				
Maximum instantaneous Forward Voltage (I)	V_F	0.51	0.51	Volts
at 7.5 Amp, Tc 125°C		0.72	0.72	
at 15 Amp, Tc 125°C		0.72	0.72	
at 15 Amp, Tc 25°C		0.64	0.64	
Maximum instantaneous Reverse Current (I)	I_R	15	15	mA
at Rated Voltage, Tc 125°C		0.1	0.1	
at Rated Voltage, Tc 25°C		0.1	0.1	

† Pulse Test: Pulse Width 30 us, Duty Cycle 20%

FIGURE 1 — TYPICAL FORWARD VOLTAGE

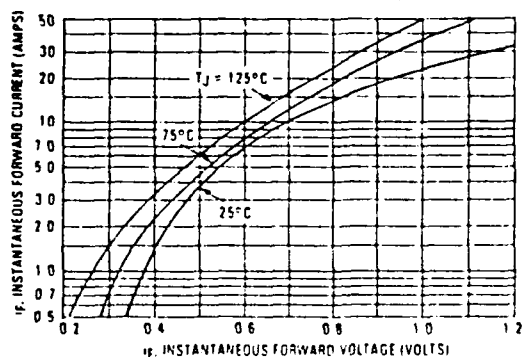


FIGURE 2 — TYPICAL REVERSE CURRENT

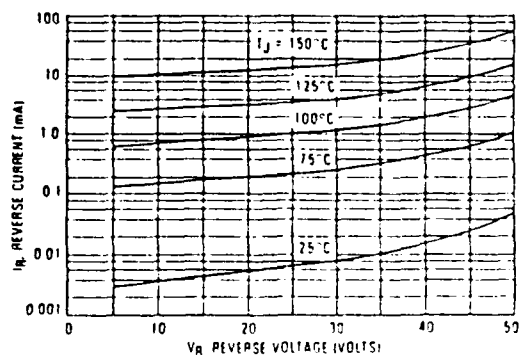


FIGURE 3 — CURRENT DERATING, CASE

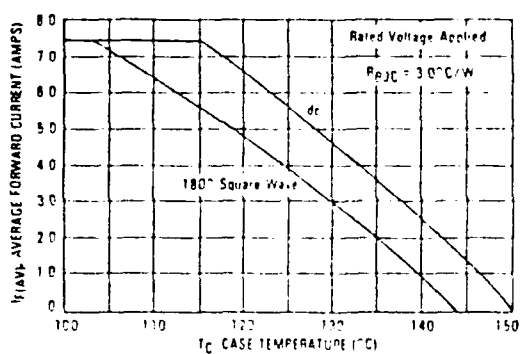


FIGURE 4 — CURRENT DERATING, AMBIENT

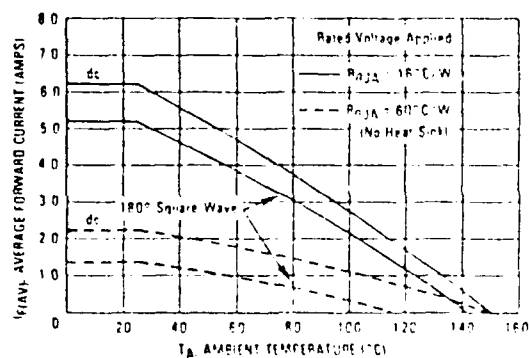
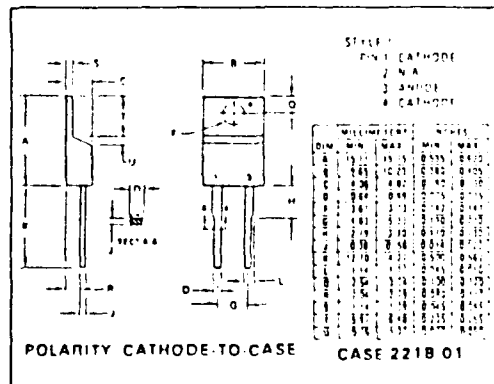
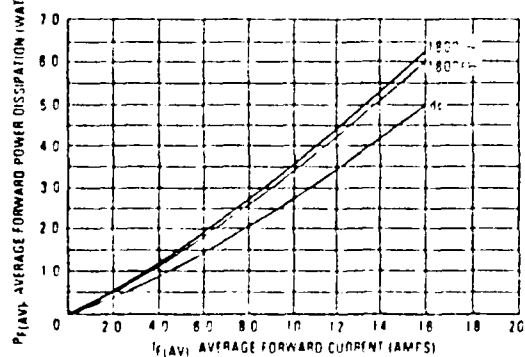


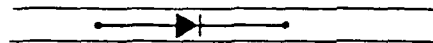
FIGURE 5 — POWER DISSIPATION



2. UltraFast [From Ref. 50]

DIODE
CONDUCTOR
ICAL DATA

MUR405 MUR450
MUR410 MUR460
MUR415 MUR470
MUR420 MUR480
MUR430 MUR490
MUR440 MUR4100



SWITCHMODE POWER RECTIFIERS

... designed for use in switching power supplies, inverters and as free wheeling diodes, these state-of-the-art devices have the following features:

- Ultrafast 25, 50 and 75 Nanosecond Recovery Times
- 175°C Operating Junction Temperature
- Low Forward Voltage
- Low Leakage Current
- High Temperature Glass Passivated Junction
- Reverse Voltage to 1000 Volts

ULTRAFast RECTIFIERS

40 AMPERES
50-1000 VOLTS



CASE 267-02
PLASTIC

MAXIMUM RATINGS

Rating	Symbol	MUR												Unit
		405	410	415	420	430	440	450	460	470	480	490	4100	
Peak Repetitive Reverse Voltage	V_{RRM}	50	100	150	200	300	400	500	600	700	800	900	1000	Volts
Working Peak Reverse Voltage	V_{RWM}													
DC Blocking Voltage	V_R													
Average Rectified Forward Current (Square Wave) (Mounting Method #3 Per Note 1)	I_{FAV}	4.0 @ $T_A = 80^{\circ}C$			4.0 @ $T_A = 40^{\circ}C$			4.0 @ $T_A = 25^{\circ}C$						Amps
Nonrepetitive Peak Surge Current (Surge applied at rated load conditions halfwave, single phase, 60 Hz)	I_{FSM}	125			70									Amps
Operating Junction Temperature and Storage Temperature	T_J, T_{stg}	- 55 to + 175												$^{\circ}C$

THERMAL CHARACTERISTICS

Maximum Thermal Resistance, Junction to Ambient	R_{JA}	See Note 1												$^\circ C/W$
---	----------	------------	--	--	--	--	--	--	--	--	--	--	--	--------------

ELECTRICAL CHARACTERISTICS

Maximum Instantaneous Forward Voltage (1) ($I_F = 3.0$ Amp, $T_J = 150^\circ C$) ($I_F = 3.0$ Amp, $T_J = 25^\circ C$) ($I_F = 4.0$ Amp, $T_J = 25^\circ C$)	V_F	0.710 0.875 0.890	1.05 1.25 1.28	1.53 1.75 1.85	Volts
Maximum Instantaneous Reverse Current (1) (Rated dc Voltage, $T_J = 150^\circ C$) (Rated dc Voltage, $T_J = 25^\circ C$)	I_R	150 5.0	250 10	900 25	μA
Maximum Reverse Recovery Time ($I_F = 1.0$ Amp, $dI/dt = 50$ Amp/ μs) ($I_F = 0.5$ Amp, $I_R = 1.0$ Amp, $t_{REC} = 0.25$ Amp)	t_{rr}	35 25	75 50	100 75	ns
Maximum Forward Recovery Time ($I_F = 1.0$ A, $dI/dt = 100$ A/ μs , Recovery to 1.0 V)	t_{fr}	25	50	75	ns

(1) Pulse Test: Pulse Width = 300 μs , Duty Cycle = 2.0%

MUR405, 410 AND 415

FIGURE 1 — TYPICAL FORWARD VOLTAGE

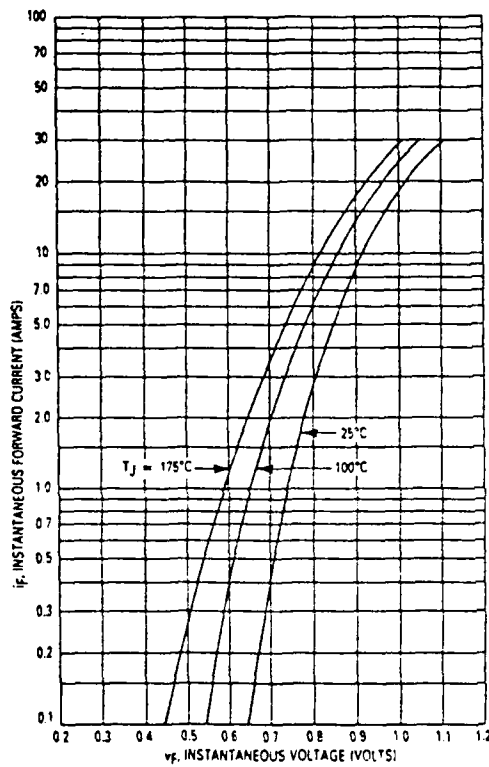


FIGURE 2 — TYPICAL REVERSE CURRENT*

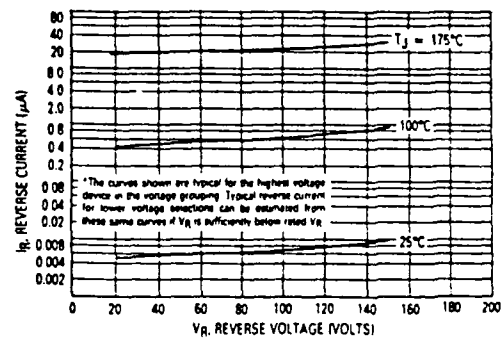


FIGURE 3 — CURRENT DERATING (MOUNTING METHOD #3 PER NOTE 1)

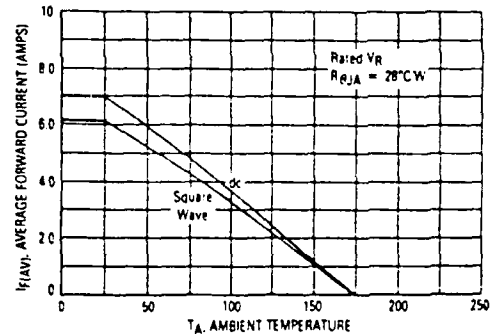


FIGURE 4 — POWER DISSIPATION

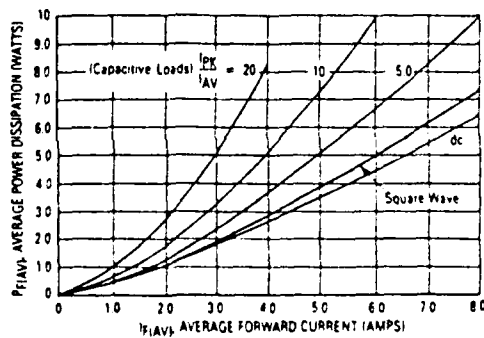
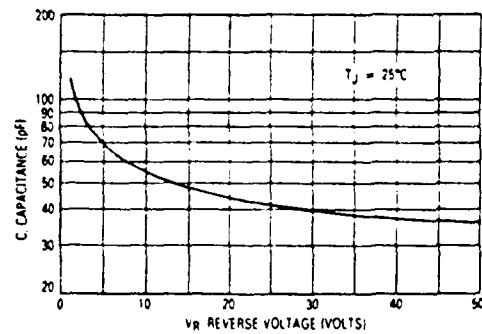


FIGURE 5 — TYPICAL CAPACITANCE



MUR405 Series

NOTE 1 — AMBIENT MOUNTING DATA

Data shown for thermal resistance junction-to-ambient ($R_{\theta JA}$) for the mountings shown is to be used as typical guideline values for preliminary engineering or in case the tie point temperature cannot be measured.

TYPICAL VALUES FOR $R_{\theta JA}$ IN STILL AIR

MOUNTING METHOD		LEAD LENGTH, L (IN)				UNITS
		1/8	1/4	1/2	3/4	
1	$R_{\theta JA}$	50	51	53	55	$^{\circ}\text{C/W}$
2		58	59	61	63	$^{\circ}\text{C/W}$
3		28				$^{\circ}\text{C/W}$

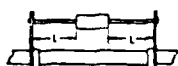
MOUNTING METHOD 1

P.C. Board Where Available Copper Surface area is small.



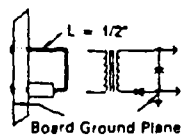
MOUNTING METHOD 2

Vector Push-In Terminals T-28



MOUNTING METHOD 3

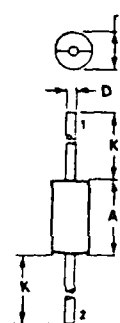
P.C. Board with 1-1/2" x 1-1/2" Copper Surface



MECHANICAL CHARACTERISTICS

Case: Transfer Molded Plastic
Finish: External Leads are Plated, Leads are readily Solderable
Polarity: Indicated by Cathode Band
Weight: 1.1 Grams (Approximately)
Maximum Lead Temperature for Soldering Purposes:
300°C, 1/8" from case for 10 s

OUTLINE DIMENSIONS



STYLE 1
PIN 1 CATHODE
2 ANODE

- NOTES
1. DIMENSIONING & TOLERANCING PER
ANSI Y14.5 1982
2. CONTROLLING DIMENSION INCH

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	9.25	—	0.37
B	—	8.35	—	0.33
C	1.22	1.32	0.048	0.052
D	25.40	—	1.000	—

CASE 267-02
PLASTIC

APPENDIX E: GATE DRIVE CIRCUIT FOR BUCK/ZCS, QUASI-RESONANT DC-DC CONVERTER

PARTS LIST

Transformer

Magnetic Circuit Elements Inc., 0-1618T2, Turns Ratio $\pm 2\%$, DCR $\pm 20\%$

Primary (5-1): 20 Turns #32 AWG

Secondary (2-6): 20 Turns #32 AWG

Transistors

Q_1 - High-Speed Switching Transistor, Silicon PNP, CGGJTX 2N3636 K8314 (f_T = 200 MHz)

Q_2 - High-Speed Switching Transistor, Silicon NPN, TI 2N3252 210 (f_T = 200 MHz)

Capacitors

C_A - Sprague 225P, 1.0 $\pm 10\%$ - 75 DC

C_B - 0.001K, X5E, 1 kV

C_C - +80-20%, 50 V, ZSV

Resistors

R_G - 10 $\Omega \pm 5\%$

Support Equipment

DC Power Supply - HP 6215A, 0 ~ 50 V (60 V_{MAX}), 250 mA

Textronik 2213 60 MHz Oscilloscope

20 MHz Pulse Function Generator Model 145 Hewlett Packard

APPENDIX F: CLASS B OUTPUT STAGE DATA SHEETS

Transformer & Inductor Specifications [From Ref. 49]

GENERAL

REFERENCE SPECIFICATIONS AND DRAWINGS CYBERDATA	DATE 7-13-38	Part No. 0-1618T2
--	-----------------	----------------------

ELECTRICAL

SCHEMATIC DIAGRAM—VOLTAGES, CURRENTS, FREQUENCY, TOLERANCES, IMPEDANCES (SOURCE, INPUT, LOAD), WINDINGS, TAPS, POLARITIES, SHIELDING, ETC.			
WINDING	URNS RATIO $\pm 2\%$	DCR $\pm 20\%$	5
5 - 1	1.000 (Ref)		20T #32
2 - 6	1.000		1
			20T #32
			6
XXXXXXXXXXXX Inductance At Terminals (5 - 1) Shall be: MAX.) MA. AV. A.C. MIN.) HENRIES $\times 10^{-3}$ Measured at 1 VOLTS 1000 CPS.			
PHASE SHIFT	FREQUENCY RESPONSE	HARMONIC DISTORTION	DUTY CYCLE
CAPACITANCE	TEST VOLTAGE @ 60 Hz 3750 VAC RMS For V.D.E	INS IMPEDANCE	TEMPERATURE RISE
PACKAGING			

OUTLINE DRAWING—CASE & MOUNTING DIMENSIONS TERMINALS IDENTIFICATION, FINISH			
1 5 9 0 6 0 2 6			
.023 SQ. PIN, TIN PLATED PHOSPHOR BRONZE, 6 PLCS			

ENVIRONMENT

TEMPERATURE RANGE	TEMPERATURE STABILITY	SHOCK	VIBRATION
ALTITUDE	HUMIDITY	LIFE	

MAGNETIC CIRCUIT ELEMENTS INC.

1540 MOFFETT ST.
SALINAS, CA 93805
PHONE: (408) 757-8752

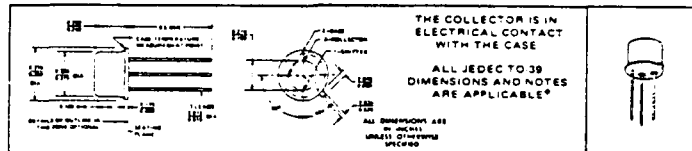
2N3252 NPN Silicon Transistors [From Ref. 51]

TYPES 2N3252, 2N3253 N-P-N SILICON TRANSISTORS

BULLETIN NO. DL 5737436 MARCH 1965—REVISED MARCH 1973

DESIGNED FOR HIGH-SPEED, HIGH-CURRENT SWITCHING APPLICATIONS

mechanical data



absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

	2N3252	2N3253
Collector-Base Voltage	60 v*	75 v*
Collector-Emitter Voltage (See Note 1)	30 v*	40 v*
Emitter-Base Voltage	5 v*	5 v*
Collector Current	1 a*	1 a*
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 2)	1 w*	1 w*
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	10 w*	5 w*
Storage Temperature	-65°C to +200°C*	-65°C to +200°C*
Lead Temperature 1/8 inch from Case for 60 Seconds	300°C*	300°C*

*electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N3252		2N3253		UNIT
		MIN	MAX	MIN	MAX	
$V_{CE(sat)}$ Collector-Base Breakdown Voltage	$I_C = 10 \text{ mA}$, $I_B = 0$	80	75	75	75	v
$V_{CE(sat)}$ Collector-Emitter Breakdown Voltage	$I_C = 10 \text{ mA}$, $I_B = 0$ See Note 4	30	40	40	40	v
$V_{BE(sat)}$ Emitter-Base Breakdown Voltage	$I_E = 10 \text{ mA}$, $I_C = 0$	5	5	5	5	v
$I_{C(sat)}$ Collector Current	$V_{CE} = 40 \text{ v}$, $I_B = 0$	0.5	0.5	0.5	0.5	a
$I_{C(sat)}$ Collector Current	$V_{CE} = 40 \text{ v}$, $I_B = 0$, $T_A = 100^\circ\text{C}$	0.5	0.5	0.5	0.5	a
$I_{C(sat)}$ Collector Current	$V_{CE} = 40 \text{ v}$, $I_B = 0$, $T_A = 100^\circ\text{C}$	0.5	0.5	0.5	0.5	a
$I_{C(sat)}$ Collector Current	$V_{CE} = 40 \text{ v}$, $I_B = 4 \text{ v}$	0.5	0.5	0.5	0.5	a
$I_{B(sat)}$ Base Current	$V_{CE} = 40 \text{ v}$, $I_C = 4 \text{ v}$	-0.5	-0.5	-0.5	-0.5	a
$I_{E(sat)}$ Emitter Current	$V_{CE} = 40 \text{ v}$, $I_C = 4 \text{ v}$	-0.5	-0.5	-0.5	-0.5	a
$I_{E(sat)}$ Emitter Current	$V_{CE} = 40 \text{ v}$, $I_C = 4 \text{ v}$	-0.5	-0.5	-0.5	-0.5	a
β_{DC} Static Forward Current Transfer Ratio	$I_C = 10 \text{ mA}$, $I_B = 100 \text{ mA}$ See Note 5	10	10	10	10	
β_{AC} Static Forward Current Transfer Ratio	$I_C = 10 \text{ mA}$, $I_B = 100 \text{ mA}$ See Note 5	10	10	10	10	
V_{BE} Base-Emitter Voltage	$I_C = 10 \text{ mA}$, $I_B = 100 \text{ mA}$ See Note 5	0.7	0.7	0.7	0.7	v
V_{BE} Base-Emitter Voltage	$I_C = 10 \text{ mA}$, $I_B = 100 \text{ mA}$ See Note 5	0.7	0.7	0.7	0.7	v
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_C = 10 \text{ mA}$, $I_B = 100 \text{ mA}$ See Note 5	0.2	0.2	0.2	0.2	v
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_C = 10 \text{ mA}$, $I_B = 100 \text{ mA}$ See Note 5	0.2	0.2	0.2	0.2	v
f_T Transition Frequency	$V_{CE} = 10 \text{ v}$, $I_C = 10 \text{ mA}$ See Note 5	250	250	250	250	Hz
C_{in} Common Base Input Capacitance	$V_{CE} = 10 \text{ v}$, $I_C = 10 \text{ mA}$ See Note 5	15	15	15	15	pF
C_{out} Common Base Output Capacitance	$V_{CE} = 10 \text{ v}$, $I_C = 10 \text{ mA}$ See Note 5	15	15	15	15	pF

- NOTES:
1. This value applies between 0 and 1 a collector current when the base-emitter diode is open-circuited.
 2. Derate linearly to 200°C free-air temperature at the rate of 5.71 mW/°C.
 3. Derate the 10-watt rating linearly to 200°C case temperature at the rate of 5.71 mW/°C. Derate the 5-watt JEDEC registered rating linearly to 200°C case temperature at the rate of 28.6 mW/°C.
 4. These parameters must be measured using pulse techniques: PW = 300 μ s, Duty Cycle \leq 2%.
 5. To obtain f_T , the f_{β} response with frequency is extrapolated at the rate of -6 dB per octave from $f = 100 \text{ Mc}$ to the frequency at which $|f_{\beta}| = 1$.
- JEDEC registered outline for these devices is TO-18 TO-39 falls within TO-18 with the exception of lead length.
- JEDEC registered data. This data sheet contains all applicable JEDEC registered data in effect at the time of publication.
- This device is qualified by Texas Instruments in addition to the JEDEC registered values which are also shown.

USES CHIP N13

TYPES 2N3252, 2N3253 N-P-N SILICON TRANSISTORS

*switching characteristics at 25°C free-air temperature

PARAMETER	TEST CONDITIONS†	2N3252	2N3253	UNIT
		MAX	MAX	
t_d Delay Time	$I_C = 500 \text{ ma}$, $I_{B1} = 50 \text{ ma}$, $V_{CE(sat)} = -2 \text{ v}$, $R_L = 59 \Omega$, See Figure 1	15	15	nsec
t_r Rise Time	$I_C = 500 \text{ ma}$, $I_{B1} = -I_{B2} = 50 \text{ ma}$, $R_L = 59 \Omega$, See Figure 2	30	35	nsec
t_s Storage Time	$I_C = 500 \text{ ma}$, $I_{B1} = -I_{B2} = 50 \text{ ma}$, $R_L = 59 \Omega$, See Figure 2	40	40	nsec
t_f Fall Time	$I_C = 500 \text{ ma}$, $I_{B1} = 50 \text{ ma}$, See Figure 3	30	30	nsec
Q_s Total Control Charge	$I_C = 500 \text{ ma}$, $I_{B1} = 50 \text{ ma}$	5	5	nCb

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

*PARAMETER MEASUREMENT INFORMATION

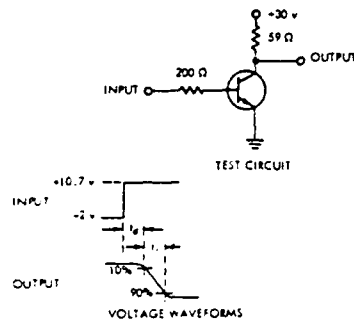


FIGURE 1 — DELAY AND RISE TIMES

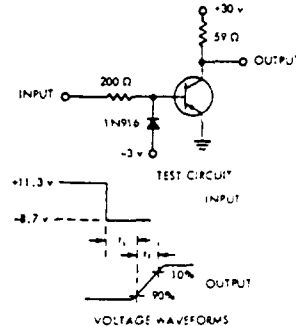
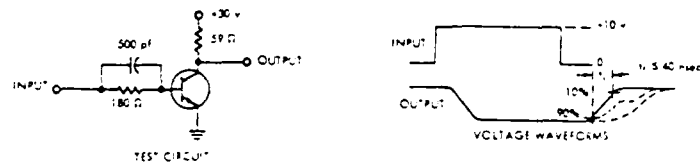


FIGURE 2 — STORAGE AND FALL TIMES



NOTE: $Q_s < 5 \text{ nCb}$ when the transistor turns off monotonically as shown by the solid line.

FIGURE 3 — TOTAL CONTROL CHARGE

NOTES: a. The input waveforms have the following characteristics:

For measuring delay and rise times: $t_r \leq 2 \text{ nsec}$, $PW \geq 200 \text{ nsec}$, Duty Cycle $\leq 2\%$.

For measuring storage and fall times: $t_r \leq 5 \text{ nsec}$, $PW \geq 10 \text{ to } 500 \text{ nsec}$, Duty Cycle $\leq 2\%$.

For measuring Q_s : $t_r \leq 10 \text{ nsec}$, $PW \geq 10 \text{ nsec}$, Duty Cycle $\leq 2\%$.

b. Waveforms are measured on an oscilloscope with the following characteristics: $t_r \leq 1 \text{ nsec}$, $B_w \geq 100 \text{ MC}$, $C_{in} \leq 7 \text{ pF}$.

*Indicates JEDEC registered data.

2N3636 PNP Silicon Transistors [From Ref. 51]

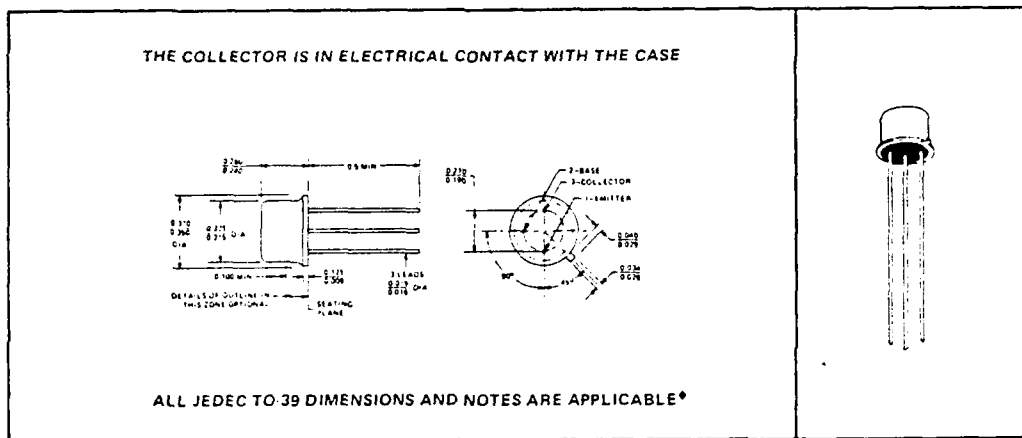
TYPES 2N3634 THRU 2N3637 P-N-P SILICON TRANSISTORS

BULLETIN NO. DL-S 7311934, JUNE 1973

HIGH-VOLTAGE TRANSISTORS FOR GENERAL PURPOSE AMPLIFIER AND SWITCHING APPLICATIONS

- High $V_{(BR)CEO}$. . . 140 V (2N3634, 2N3635) or 175 V (2N3636, 2N3637)
- High Dissipation Capability . . . 10 W at 25°C Case Temperature

mechanical data



absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

	2N3634	2N3636
	2N3635	2N3637
Collector-Base Voltage	-140 V*	-175 V*
Collector-Emitter Voltage (See Note 1)	-140 V*	-175 V*
Emitter-Base Voltage	-5 V*	-5 V*
Continuous Collector Current	1 A*	1 A*
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 2)	10 W†	10 W†
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	5 W*	5 W*
Storage Temperature Range	-65°C to 200°C*	-65°C to 200°C*
Lead Temperature 1/16 Inch from Case for 10 Seconds	300°C†	240°C*

NOTES 1 These values apply between 0 and 10 mA collector current when the emitter-base diode is open-circuited.

2 Derate linearly to 200°C free-air temperature at the rate of 5.71 mW/°C.

3 Derate the 10-watt rating linearly to 200°C case temperature at the rate of 57.1 mW/°C. Derate the 5-watt (JEDEC registered) rating linearly to 200°C case temperature at the rate of 28.6 mW/°C.

*The JEDEC registered outline for these devices is TO-5. TO-39 falls within TO-5 with the exception of lead length.

†JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

‡These values are guaranteed by Texas Instruments in addition to the JEDEC registered values which are also shown.

TYPES 2N3634 THRU 2N3637
P-N-P SILICON TRANSISTORS

*electrical characteristics at 25°C free-air temperature

PARAMETER	TEST CONDITIONS	2N3634		2N3635		2N3636		2N3637		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V _{(BR)CBO} Collector-Base Breakdown Voltage	I _C = -100 μ A, I _E = 0	-140		-140		-175		-175		V
V _{(BR)CEO} Collector-Emitter Breakdown Voltage	I _C = -10 mA, I _B = 0, See Note 4	-140		-140		-175		-175		V
V _{(BR)EBO} Emitter-Base Breakdown Voltage	I _E = -10 μ A, I _C = 0	-5		-5		-5		-5		V
I _{CBO} Collector Cutoff Current	V _{CB} = -100 V, I _E = 0	-100		-100		-100		-100		nA
I _{EBO} Emitter Cutoff Current	V _{EB} = -3 V, I _C = 0	-50		-50		-50		-50		nA
h _{FE} Static Forward Current Transfer Ratio	V _{CE} = -10 V, I _C = -0.1 mA	40		80		40		80		
	V _{CE} = -10 V, I _C = -1 mA	45		90		45		90		
	V _{CE} = -10 V, I _C = -10 mA	See Note 4	50	100		50		100		
	V _{CE} = -10 V, I _C = -50 mA	50	150	100	300	50	150	100	300	
	V _{CE} = -10 V, I _C = -150 mA	25		50		25		50		
V _{BE} Base-Emitter Voltage	I _C = -10 mA, I _B = -1 mA	See Note 4	-0.8		-0.8		-0.8		-0.8	V
	I _C = -50 mA, I _B = -5 mA	-0.65	-0.9	-0.65	-0.9	-0.65	-0.9	-0.65	-0.9	
V _{CE(sat)} Collector-Emitter Saturation Voltage	I _C = -10 mA, I _B = -1 mA	See Note 4	-0.3		-0.3		-0.3		-0.3	V
	I _C = -50 mA, I _B = -5 mA	-0.5		-0.5		-0.5		-0.5		
h _{ie} Small-Signal Common-Emitter Input Impedance	V _{CE} = -10 V, I _C = -10 mA, f = 1 kHz	0.1	0.6	0.2	1.2	0.1	0.6	0.2	1.2	k Ω
h _{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio		40	160	80	320	40	160	80	320	
h _{re} Small-Signal Common-Emitter Reverse Voltage Transfer Ratio		3 \times 10 ⁻⁴		3 \times 10 ⁻⁴		3 \times 10 ⁻⁴		3 \times 10 ⁻⁴		
h _{oe} Small-Signal Common-Emitter Output Admittance		200		200		200		200		μ mho
h _{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	V _{CE} = -30 V, I _C = -30 mA, f = 100 MHz	1.5		2		1.5		2		
C _{obo} Common-Base Open-Circuit Output Capacitance	V _{CB} = -20 V, I _E = 0, f = 100 kHz		10		10		10		10	pF
C _{ibo} Common-Base Open-Circuit Input Capacitance	V _{EB} = -1 V, I _C = 0, f = 100 kHz		75		75		75		75	pF

NOTE 4: These parameters must be measured using pulse techniques: t_w = 300 μ s, duty cycle \leq 2%.

TYPES 2N3634 THRU 2N3637 P-N-P SILICON TRANSISTORS

*operating characteristics at 25°C free-air temperature

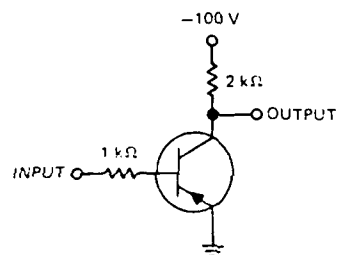
PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
F Spot Noise Figure	$V_{CE} = -10 \text{ V}$, $I_C = -0.5 \text{ mA}$, $R_G = 1 \text{ k}\Omega$, $f = 1 \text{ kHz}$		3	dB

*switching characteristics at 25°C free-air temperature

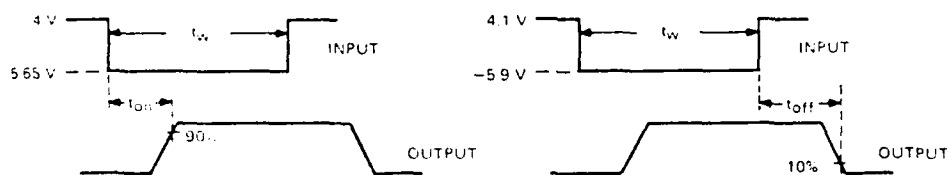
PARAMETER	TEST CONDITIONS†	MIN	MAX	UNIT
t_{on} Turn-On Time	$V_{CC} = -100 \text{ V}$, $I_C = -50 \text{ mA}$, $I_{B(1)} = -5 \text{ mA}$, $V_{BE(off)} = 4 \text{ V}$, See Figure 1		400	ns
t_{off} Turn-Off Time	$V_{CC} = -100 \text{ V}$, $I_C = -50 \text{ mA}$, $I_{B(1)} = -5 \text{ mA}$, $I_{B(2)} = 5 \text{ mA}$, See Figure 1		600	ns

† Voltage and current values shown are nominal, exact values vary slightly with transistor parameters.

*PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 1

NOTES A The input waveforms are supplied by a generator with the following characteristics: $Z_{out} = 50 \Omega$, $t_r \leq 20 \text{ ns}$, $t_f \leq 20 \text{ ns}$, $t_w \approx 20 \mu\text{s}$, duty cycle $\leq 2\%$.
B Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 10 \text{ ns}$, $R_{in} \geq 100 \text{ k}\Omega$, $C_{in} \leq 5 \text{ pF}$.

† DEC registered data

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